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Mitsubishi Electric Research Laboratories, Inc.
201 Broadway, Cambridge, Massachusetts 02139

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Yicong Dong, Eiji Yagyu, Takashi Matsuda, Chungwei Lin, Shaloo Rakheja, *Senior Member, IEEE*

***Abstract*—This work presents a compact-model-based delay analysis of a 0.5-μm gate-length GaN HEMT using small-signal parameters extracted from the MIT Virtual Source GaNFET-RF model. The delay framework separates the contributions of the intrinsic channel, extrinsic channel, and parasitic elements associated with access resistance and gate-to-drain Miller capacitance over a baseplate temperature range of 298–423 K. The results show that the total delay is dominated by the extrinsic channel, attributed to fringing-field coupling from the T-gate sidewalls, while parasitic delay contributes less than 13% of the total delay. This indicates that cutoff-frequency improvement is more likely to come from gate geometry and channel electrostatic optimization than from access-region resistance reduction alone. The cutoff frequency degrades at approximately 0.2%/K, primarily due to reduced transconductance and increased intrinsic gate-to-source capacitance at elevated temperature. These results provide a quantitative link between layout-dependent delay components, thermal degradation, and RF performance in GaN HEMTs.**

***Index Terms*—GaN HEMT, MVSG compact model, delay time analysis, thermal robustness, small-signal model**

I. Introduction

GALLIUM NITRIDE (GaN) high-electron-mobility transistors (HEMTs) have emerged as a leading technology for high-power and high-frequency applications [1], [2], where operation under elevated thermal loads is often unavoidable [3], [4]. A key figure of merit for such devices is the cutoff frequency, f_{T}, defined as the frequency at which the current gain drops to unity [5]. While high f_{T} is a central target in GaN HEMT design, maintaining this performance at elevated ambient or baseplate temperatures remains a critical challenge for high-power RF operation [6].

Understanding the temperature dependence of f_{T} requires more than tracking its overall degradation; it requires identifying which delay components are most sensitive to temperature. In particular, decomposing the total delay into intrinsic, extrinsic, and parasitic contributions [7], [8] provides a direct way to connect thermal degradation to the underlying device physics, including changes in transconductance, capacitance, access resistance, and channel charge distribution. Such analysis can reveal whether elevated temperature primarily degrades the gated-channel response, the access regions, or the extrinsic terminal capacitances.

This delay-based perspective also provides guidance for device optimization. If parasitic or extrinsic delays dominate, improvements may be pursued through source/drain access-region engineering and reduction of geometry-dependent parasitic capacitances and resistances. Conversely, if f_{T} is limited primarily by intrinsic delay, gate-length scaling becomes the more direct route for performance improvement, provided that the top- and back-barrier designs are co-optimized to suppress short-channel effects and preserve electrostatic control [9]. Therefore, temperature-dependent delay analysis not only clarifies the physical origin of RF performance degradation, but also identifies the most relevant design pathways for improving the thermal robustness of GaN HEMTs.

In this work, we analyze the delay characteristics by extracting the Massachusetts Institute of Technology (MIT) Virtual Source GaNFET-RF (MVSG-RF) compact model `version` 1.1.0 [10] for a GaN HEMT fabricated and experimentally characterized from 298 K to 423 K, at Mitsubishi Electric Corporation [11]. The device's DC

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Y. Dong (e-mail: yicongd2@illinois.edu) and S. Rakheja (e-mail: rakheja@illinois.edu) are with the Holonyak Micro and Nanotechnology Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801.

E. Yagyu (e-mail: Yagyu.Eiji@cb.MitsubishiElectric.co.jp) and T. Matsuda (e-mail: Matsuda.Takashi@dn.MitsubishiElectric.co.jp) are with the Mitsubishi Electric Corporation, Amagasaki 661-8661, Japan

C. Lin (e-mail: clin@merl.com) is with the Mitsubishi Electric Research Laboratories, Cambridge, MA 02139.

characteristics was also previously simulated in TCAD (Sentaurus from Synopsys) and calibrated against measurement data from 298 K to 423 K [11]. The model is calibrated against DC and small-signal measurements to ensure accurate representation of device behavior. Using the extracted model, we demonstrate design iterations and predict the small-signal performance of the HEMT under elevated baseplate temperatures and scaled access region lengths. We show that aggressive access-region scaling alone produces only modest improvement in f_{T}. Drain-access scaling weakly reduces intrinsic delay through channel charge repartitioning, whereas source-access scaling improves transconductance, but simultaneously increases the intrinsic gate-to-source capacitance, limiting the net gain. Elevated baseplate temperature degrades f_{T} primarily through the reduction of transconductance, with additional sensitivity arising from temperature-dependent changes in channel charge and the associated intrinsic gate-to-source capacitance.

Temperature-dependent RF performance and reliability of GaN HEMTs have been extensively investigated, including under prolonged electrical stress and elevated channel temperatures [12]. Such studies primarily address the degradation mechanisms and reliability of devices under severe operating conditions. The objective of the present work is complementary: rather than investigating stress-induced degradation, we seek to identify the physical origins of f_{T} limitation of an experimentally fabricated GaN HEMT technology under small-signal RF operation. By decomposing the total transistor delay into its constituents along with thermally aware device physics, our work connects the isolated device-level design choices directly to the small-signal RF limit, f_{T}, of a fabricated AlGaN/GaN HEMT.

The present analysis is intended to quantify device-level small-signal cutoff-frequency limitations rather than the complete large-signal behavior of a packaged RF power transistor. Even though our present study is limited to the small-signal regime, small-signal analysis has its own value that it provides a physically meaningful assessment of the device's terminal response, current-gain, effective charging/transit time, and high-frequency performance limiting components around each quiescent point; and it guides us with clearer future directions to look for in the large-signal domain. Package-, board-, and circuit-level parasitics, as well as the detailed thermal resistance from the device through the package and heat sink can substantially affect the realized RF performance of a fabricated device or MMIC, but they also depend strongly on the specific implementation and are beyond the scope of the present study thus not the focus of our work.

II. Fabrication and Model Calibration

A. Device Structure and Fabrication

The AlGaN/GaN HEMT, as shown in Fig. 1, is fabricated through a multi-step process. GaN epitaxial layers are first deposited on SiC substrates by metal–organic chemical vapor deposition (MOCVD). Device isolation is implemented using argon ion implantation. Ohmic source and drain regions are formed by Si implantation followed by an activation anneal, after which gate metal stacks are deposited via electron beam evaporation and subjected to rapid thermal annealing. These metallization steps are patterned using standard photolithography and lift-off procedures. Gate formation is carried out by using i-line stepper exposure and chemical shrink process technique [13]. As a final step, a silicon nitride (Si_3N_4) passivation layer is deposited by CVD to improve device reliability and electrical performance.

The fabricated device consists of an asymmetric GaN channel where the T-shaped gate sits closer to the source. The T-shaped gate reduces the gate contact resistance while shortening channel length [14], and the asymmetric channel improves breakdown strength on the drain access side [15], [16]. The GaN cap reduces both gate lag, via improved surface control [17], and off-state leakage through the Schottky barrier [18] but is not modeled in the MVSG-RF 1.1.0 for simplicity. In addition to the gate, drain and source contacts, a body contact is present but not shown, and a multi-step source field plate (SFP) design is added for better electrostatic control [19]. Gate length L (`l`), source access length L_{gs} (`lgs`) and drain access length L_{gd} (`lgd`) are approximately 0.5, 1.3 and 3.8 µm, respectively. The exact dimensions are not disclosed for intellectual property reasons.

The MVSG-RF 1.1.0 model only implements field plates as implicit transistors on the drain side of the intrinsic gated transistor (see Fig. 4.5 in [10]). We choose to model one gate field plate `lgfp1` for the T-shaped gate and two source field plates `lgfp2` and `lgfp3` for the multi-step (see Fig. 1), with dimensions 0.24, 0.17 and 0.75 µm, respectively. The SFP introduces additional electrostatic coupling to the drain-side access region and therefore contributes to the extrinsic capacitance and associated RF delay. In the present, MVSG-RF implementation, this contribution is represented by two lumped capacitance segments associated with the SFP geometry which does not vary with scaling the access regions, *i.e.*, any change in f_{T} attributed to access scaling is evaluated with the SFP capacitive network retained consistently, rather than inadvertently changing field-plate geometry at the same time. These elements capture the principal capacitive loading of the field plate and are

retained in the delay and f_T calculations. Detailed bias-dependent redistribution of charge beneath the individual field-plate sections is not separately resolved because calibration of such contributions would require dedicated field-plate C-V structures. Thus, the present analysis includes the SFP contribution to the baseline extrinsic capacitance while treating its detailed charge distribution within a reduced-order approximation.

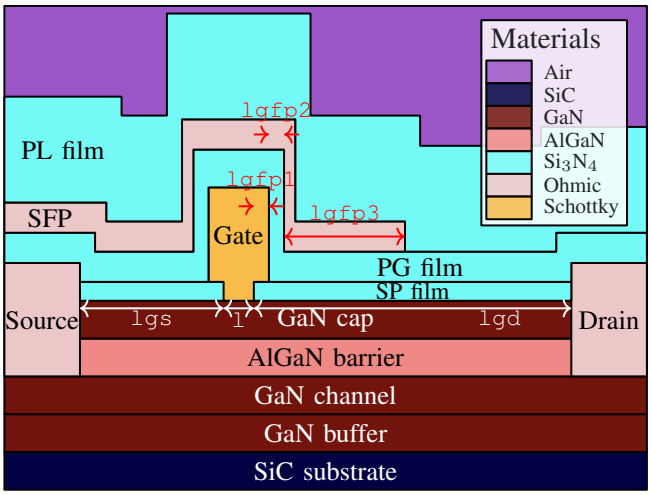


Fig. 1. Cross-section of the fabricated AlGaN/GaN HEMT with labeled material layers. Drawing is not to scale. Only dimensions relevant to the MVSG-RF compact model are labeled. SFP: source field plate, SP: silicon nitride passivation, PG: gate passivation, PL: general passivation layer.

This fabricated device exhibits peak current of 1000 mA/mm, peak transconductance of 300 mS/mm, maximum forward gate-drain leakage current of 200 mA/mm, reverse gate-drain leakage current in the order of $10^{-2} - 10^{-1}$ mA/mm at room temperature (see Supplementary Material Sec. V for measured transconductance and gate leakage profiles) [11]. Compared to similar published technology nodes at 500 nm, leakage current of this device is higher [20], [21] while peak drain output current is comparable or higher [21]–[23]. Peak transconductance is meanwhile superior compared to [21]–[23].

B. DC I-V Characteristics Calibration

The measured DC I-V characteristics include transfer curves for gate-to-source biases $V_{GS} \in [-5, 2]$ V at gate-to-drain biases $V_{DS} = \{2, 5, 10, 20\}$ V for base-plate temperatures $T_{base} = \{298, 323, 373, 423\}$ K. Measurement data also include output characteristics for $V_{DS} \in [0, 20]$ V at $V_{GS} = \{-2, -1, 0, 1, 2\}$ V and $T_{base} = \{298, 323, 373\}$ K. Off-state subthreshold transfer characteristics are used to calibrate parameters like threshold voltage (`vto`), subthreshold swing (`ss`), drain-induced barrier lowering (`delta1`), etc. On-state transfer characteristics and output characteristics are used to calibrate parameters for the intrinsic transport properties such as low-field mobility (`mu0`) and saturation velocity (`vsat`) as well as parameters for the access transport properties such as sheet resistance (`rsh`) and source access implicit gate capacitance (`cgrs`). On-state forward leakage due to thermionic emission [24] and corresponding temperature dependence parameters are obtained with $V_{GS} = 2$ V traces. The gate capacitance (`cg`) is attempted but not fully calibrated here since it requires further calibration using the C-V characteristics in Sec. II-C. Some of the DC fitting results can be found in Fig. 2 where not all calibrations are presented for simplicity. A comprehensive list of all calibrated parameters is available upon request. All measurements reported here are performed for $V_{DS} \leq 20$ V, which is well within the intended normal operating regime.

C. C-V Characteristics Calibration

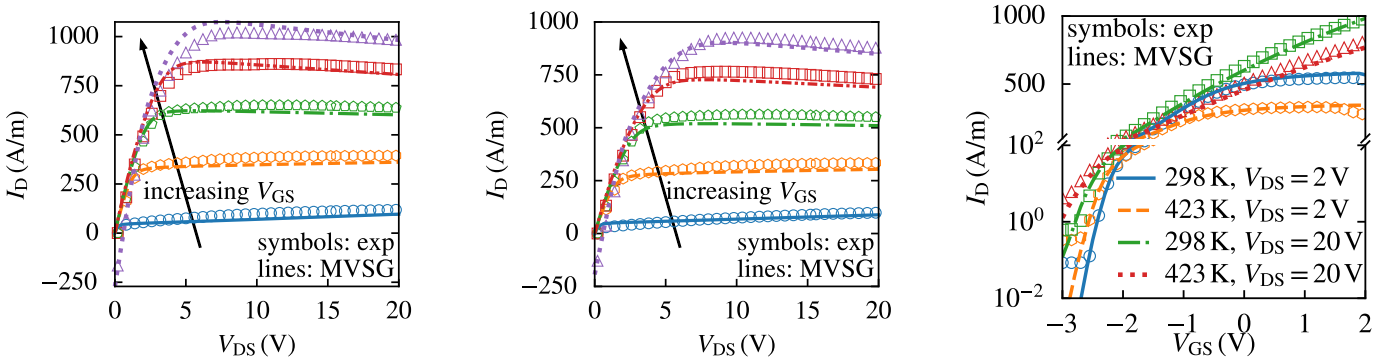
For C-V characteristics, we divide the calibration into two branches, namely the gate-to-source capacitance C_{gs} and the gate-to-drain capacitance C_{gd}. Measurements are available for $V_{DS} = \{0, 0.01, 0.5, 1, 1.5, 2, 3, 4, 5, 10\}$ V at $T_{base} = 298$ K, but we only show few of the calibrated results for conciseness in Fig. 3. In each branch of the C-V, the capacitance consists of three different components, and taking C_{gs} as an example

$$C_{gs} = C_{gs}^{int} + C_{gs}^{fring} + C_{gs}^{par}, \tag{1}$$

where C_{gs}^{int} is the intrinsic gate-to-source capacitance due to gated channel charges and is partially determined by the aforementioned `cg`, C_{gs}^{fring} is the gate-to-source fringing capacitance further consisting of inner fringing C_{gs}^{if} (`cifms`) and outer fringing C_{gs}^{of} (`cofsm`), and C_{gs}^{par} is the parasitic gate-to-source capacitance in the form of lumped elements, further discussed in Sec. II-D. By symmetry, similar expressions can be also obtained for C_{gd}. Therefore, combining C-V and DC I-V characteristics, we can fit to the value of `cg`, inner fringing capacitance and the sum of outer fringing and parasitic capacitance. With the help of S-parameter calibration in Sec. II-D, outer fringing and parasitic capacitance can then be separated. One slight adjustment to the MVSG-RF 1.1.0 model is that, instead of a constant gate-drain inner fringing field, we use

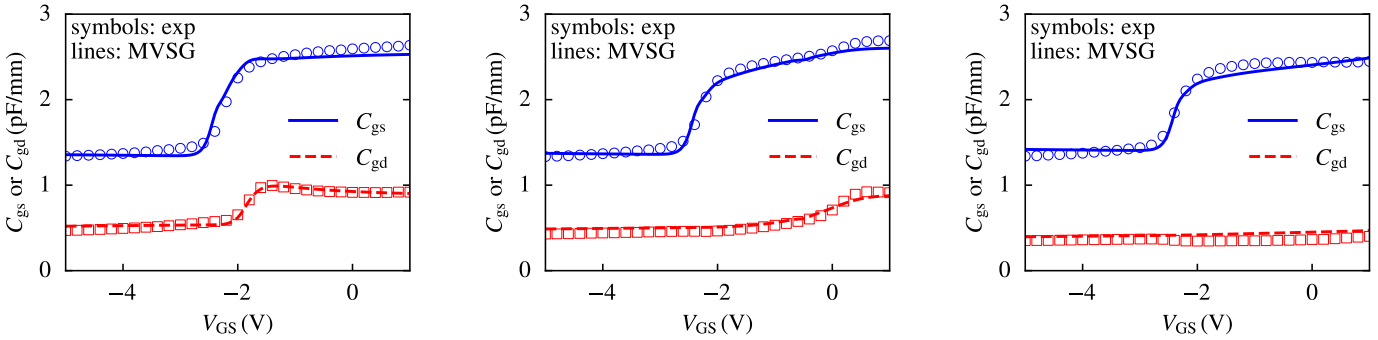
$$C_{gd}^{if} = C_{gd}^{if,0} - C_{gd}^{corr} V_{DS,i}, \tag{2}$$

where C_{gd}^{corr} is a linear voltage dependence parameter. This accounts for the experimentally observed degradation of C_{gd}^{if} at higher V_{DS}. As our simulations only reach



(a) Output curves at 298 K. (b) Output curves at 373 K. (c) Transfer curves at 298 and 423 K.

Fig. 2. Measured and simulated DC I-V characteristics at various baseplate temperatures. Output curves are for $V_{GS} = \{-2, -1, 0, 1, 2\}$ V.



(a) C-V characteristics at $V_{DS} = 0.5$ V. (b) C-V characteristics at $V_{DS} = 3$ V. (c) C-V characteristics at $V_{DS} = 10$ V.

Fig. 3. Measured and simulated C-V characteristics calibrated at 298 K.

a maximum of $V_{DS} = 30$ V, we may choose the value of C_{gd}^{corr} carefully such that no negative C_{gd}^{if}'s will occur.

C_{ds}-V_{GS} characteristics are measured but not calibrated or reported because a near constant value is found for the saturation regime of the device. Therefore, we adopt a single parasitic element to account for this branch in Sec. II-D. Body capacitances are neither measured nor calibrated because the substrate is 50-µm thick semi-insulating SiC as depicted in Fig. 1, not an electrically active backside substrate; as such, we do not expect field plates to couple with the body.

D. Small-Signal S-Parameters Calibration

For the S-parameter calibration, we first employ the hot-cold de-embedding procedure introduced in [25] to obtain initial estimates of the extrinsic parasitic elements. Using these estimates, we construct the equivalent circuit shown in Fig. 4 and extract the parasitic parameters listed in Table I at 298 K. Additional details regarding S-parameter measurements and model calibrations can be found in Supplementary Material Sec. III.

The fitted C_{pgs} and C_{pgd} parameters are assigned the same values as the corresponding de-embedded parasitic capacitances C_{gs}^{par} and C_{gd}^{par} introduced in Sec. II-C. These extrinsic capacitances are assumed to be temperature independent, consistent with a commonly adopted approximation in temperature-dependent compact modeling [26]–[30]. They determine the capacitive component of the parasitic charging/discharging delay considered below.

Some studies have nevertheless reported a finite temperature dependence of outer-fringing and other extrinsic capacitances [31], [32]. Reported coefficients for the extrinsic C_{gs} contribution are approximately -0.1 to -0.2%/K, which would correspond to a 10–20% reduction over the 298–398 K range considered here. Because elevated-temperature C-V measurements are unavailable for the present device, this dependence is not included in the calibration. If present, such a reduction would decrease the capacitance-related extrinsic delay relative to the temperature-invariant assumption and would therefore partially mitigate the predicted degradation of f_T. The impact on the total f_T is expected to be smaller than the corresponding fractional change in the extrinsic capacitance because the total delay contains multiple intrinsic, extrinsic, and parasitic contributions.

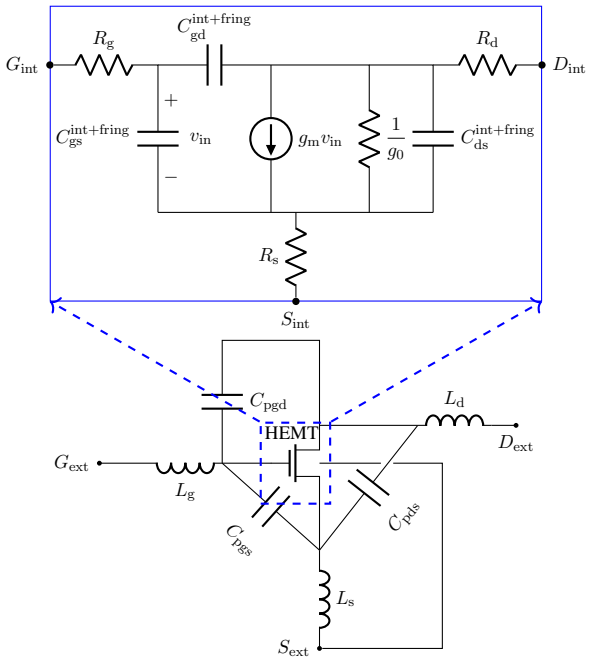
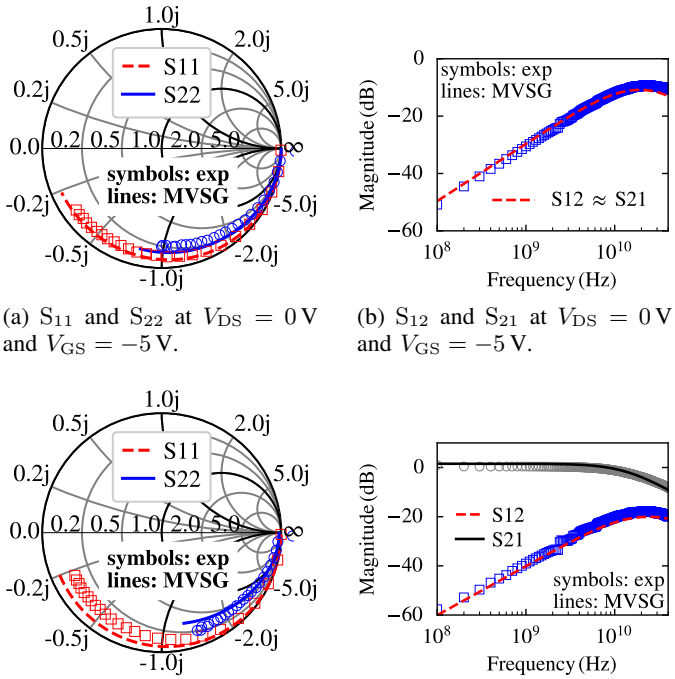


Fig. 4. Circuit schematics showing intrinsic device and lumped parasitic elements. Consult text and Table I for the meaning of various circuit elements.

TABLE I
FITTING PARAMETERS AT 298 K FOR DE-EMBEDDED PARASITIC COMPONENTS SHOWN IN FIG. 4.

Symbol	Meaning	Value
L_g	Parasitic gate inductance	25 pH
R_g	Parasitic gate resistance	1.5 Ω
L_s	Parasitic source inductance	5 pH
L_d	Parasitic drain inductance	5 pH
C_{pgs}	Parasitic gate-to-source capacitance	2×10^{-14} F
C_{pgd}	Parasitic gate-to-drain capacitance	1×10^{-14} F
C_{pds}	Parasitic drain-to-source capacitance	2.5×10^{-14} F

The drain and source contact resistances are not included in this extraction, since they have already been calibrated within the MVSG model using the measured DC characteristics. Representative S-parameter calibration results at 298 K for the hot and pinched-off cold device conditions are shown in Fig. 5. The close agreement between the measured S-parameters and those reconstructed using the extracted equivalent-circuit parameters over the measurement bandwidth provides a direct validation of the equivalent-circuit representation used for the subsequent intrinsic-parameter and delay analyses. While the agreement is not exact, particularly at higher frequencies, the model captures the relevant behavior over the frequency range of interest. Since the devices are operated well below their cutoff frequency, which is less than 10 GHz as shown in Fig. 6, deviations above 20 GHz are not expected to significantly affect the accuracy of the subsequent circuit simulations.



(a) S_{11} and S_{22} at $V_{DS} = 0$ V and $V_{GS} = -5$ V.

(b) S_{12} and S_{21} at $V_{DS} = 0$ V and $V_{GS} = -5$ V.

(c) S_{11} and S_{22} at $V_{DS} = 30$ V and $I_D = 0.015$ A, *i.e.*, $V_{GS} = -2.5$ V.

(d) S_{12} and S_{21} at $V_{DS} = 30$ V and $I_D = 0.015$ A, *i.e.*, $V_{GS} = -2.5$ V.

Fig. 5. Measured and simulated S-parameters from 0.1 GHz to 40 GHz calibrated at 298 K. See higher gate overdrive hot-device simulation results in Supplementary Material Sec. IV.

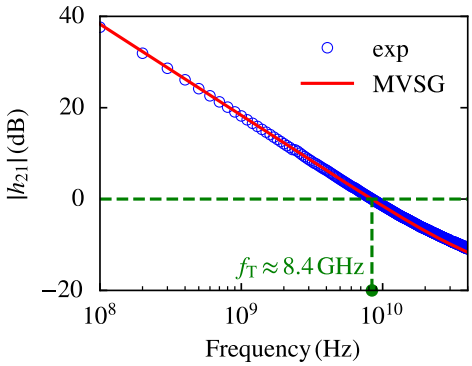


Fig. 6. Measured and simulated current gain vs. frequency calibrated at $V_{DS} = 30$ V and $I_D = 0.015$ A, *i.e.*, $V_{GS} = -2.5$ V. $f_T \approx 8.4$ GHz.

III. Device Delay and Cutoff Frequency

With the calibrated MVSG model accurately capturing the DC I-V characteristics and S-parameters of the GaN HEMT, the limits of f_T can be interpreted in terms of the underlying delay components [33]. Specifically, $f_T = 1/(2\pi\tau_t)$, where $\tau_t = \tau_{int} + \tau_{ext} + \tau_{par}$ is the total delay. Here, τ_{int} denotes the intrinsic delay

associated with carrier transport through the gated channel, $\tau_{\rm ext}$ represents the extrinsic delay associated with parasitic capacitances arising from gate fringing fields, and $\tau_{\rm par}$ captures the parasitic delay associated with the source/drain access regions, including the Miller effect due to the gate-to-drain capacitance. These delay components are given as

$$\tau_{\rm int} = \frac{C_{\rm gs}^{\rm int} + C_{\rm gd}^{\rm int}}{g_{\rm m}}, \tag{3}$$

$$\tau_{\rm ext} = \frac{C_{\rm gs}^{\rm ext} + C_{\rm gd}^{\rm ext}}{g_{\rm m}}, \tag{4}$$

$$\tau_{\rm par} = (R_{\rm s} + R_{\rm d}) \left[C_{\rm gd} + (C_{\rm gs} + C_{\rm gd}) \frac{g_0}{g_{\rm m}} \right], \tag{5}$$

where $C_{\rm gs}^{\rm ext} = C_{\rm gs}^{\rm fring} + C_{\rm gs}^{\rm par}$ is the extrinsic gate-source capacitance, likewise $C_{\rm gd}^{\rm ext} = C_{\rm gd}^{\rm fring} + C_{\rm gd}^{\rm par}$ is the extrinsic gate-drain capacitance, $R_{\rm s}$ and $R_{\rm d}$ are the source and drain access plus contact resistances, $C_{\rm gs} = C_{\rm gs}^{\rm int} + C_{\rm gs}^{\rm ext}$, likewise $C_{\rm gd} = C_{\rm gd}^{\rm int} + C_{\rm gd}^{\rm ext}$, $g_{\rm m}$ is the transconductance, and g_0 is the output conductance. This model provides clear physical insight into the design factors that limit device performance and identifies how the device geometry can be optimized to reduce the dominant delay components, thereby enhancing $f_{\rm T}$.

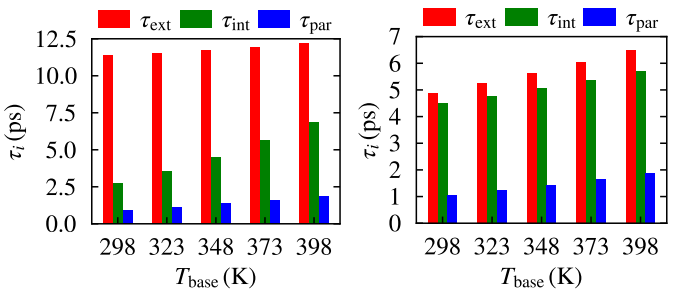
Using the extracted values of the small-signal HEMT parameters, we estimate that for our technology at 298 K and the specific bias ($V_{\rm GS} = -2.5\,{\rm V}$; $V_{\rm DS} = 30\,{\rm V}$), $\tau_{\rm int}$ contributes 18% of the total delay, $\tau_{\rm ext}$ contributes 76%, while the remainder delay is attributed to $\tau_{\rm par}$. The cutoff frequency predicted by the delay model is $10.5\,{\rm GHz}$, which, despite being higher than the $8.4\,{\rm GHz}$ estimated from S-parameters, qualitatively matches the trends with respect to access-region scaling (see Supplementary Material Sec. I) and baseplate temperature (see Sec. III-A).

The above analysis shows that the parasitic delay constitutes only a small fraction of the total delay; therefore, strategies aimed solely at reducing access-region resistance are expected to have a limited impact on the HEMT cutoff frequency. To verify this, we extracted the small-signal parameters of the GaN HEMT and estimated the cutoff frequency while scaling the access-region dimensions. The key result is that drain-access scaling provides only a modest improvement in $f_{\rm T}$. Even when $L_{\rm gd}$ is reduced by 90%, the increase in $f_{\rm T}$ remains below 10%. Both $\tau_{\rm int}$ and $\tau_{\rm par}$ decrease by less than $1\,{\rm ps}$ over the entire scaling range, while $\tau_{\rm ext}$ remains unchanged. Similar to drain-access scaling, reducing $L_{\rm gs}$ produces only a modest improvement in $f_{\rm T}$, with the maximum increase remaining close to 10% even for a 90% reduction in $L_{\rm gs}$. Additional details regarding access-region scaling can be consulted in Supplementary Material Sec. I.

A. *Temperature-sensitive delay analysis*

As seen in Sec. II, elevated-temperature measurements were performed for the DC characteristics, whereas the C–V and S-parameter measurements used for RF parameter extraction were performed at room temperature. Temperature-dependent RF characteristics and capacitances presented subsequently are therefore predictions of the calibrated MVSG-RF model rather than direct elevated-temperature RF measurements. Steady-state self-heating is included through a thermal resistance, $R_{\rm th}$. Since the extracted thermal time constant exceeds $10^{-4}\,{\rm s}$, dynamic thermal modulation is negligible over the RF frequency range considered here. Trapping and thermal transients in this technology were independently characterized previously using pulsed measurements and dynamic charge-trapping simulations [11]. Spatially resolved electrothermal effects are not considered. Package interconnects, matching networks, and circuit-level parasitics are likewise outside the scope of the device-level $f_{\rm T}$ and delay decomposition presented here.

We quantify the relative contributions of the individual delay components to the total HEMT delay at different baseplate temperatures, as shown in Fig. 7. It can be seen that all delay components increase with $T_{\rm base}$, with the most increase observed in the intrinsic delay component near threshold and in the extrinsic delay component above threshold. Moreover, the parasitic delay components remains within 13% of the overall delay across all $T_{\rm base}$ values considered here. Nonetheless, all delay components worsen with a rate of in the range of $8 - 41\,{\rm fs/K}$ temperature rise.



(a) $(V_{\rm GS}, V_{\rm DS}) = (-2.5, 30)\,{\rm V}$. (b) $(V_{\rm GS}, V_{\rm DS}) = (-1.5, 20)\,{\rm V}$.

Fig. 7. Individual delay components vs. baseplate temperatures.

Specifically, our analysis indicates that the increase in $\tau_{\rm ext}$ with $T_{\rm base}$ arises primarily from the reduction in $g_{\rm m}$ (see Fig. 8(a)), which signifies a reduction in the gate modulation speed of the channel charge. The reduction in $g_{\rm m}$ dominates over the simultaneous decrease

in $C_{\mathrm{gs}}^{\mathrm{ext}}$ (see Fig. 8(b)), particularly at $(V_{\mathrm{GS}}, V_{\mathrm{DS}}) = (-2.5, 20)\,\mathrm{V}$. As T_{base} increases from 298 K to 398 K, the low-field region beneath the source contact and in the source access region moves closer to the top of the device, indicating stronger electrostatic screening due to increased ionized charge. This behavior is not observed at $(V_{\mathrm{GS}}, V_{\mathrm{DS}}) = (-1.5, 20)\,\mathrm{V}$. In this case, the device is already turned on, and the 2DEG charge dominates the space-charge distribution. Consequently, the fringing field lines show little temperature dependence. As a result, $C_{\mathrm{gs}}^{\mathrm{ext}}$ decreases with increasing T_{base} only at $(V_{\mathrm{GS}}, V_{\mathrm{DS}}) = (-2.5, 30)\,\mathrm{V}$.

The increase in τ_{par} with T_{base} is mainly attributed to the increase in the source and drain access resistances, R_{s} and R_{d}. In this case, the effects of the decreasing g_0 (see Fig. 8(c)) and g_{m} largely offset each other, while the total C_{gs} remains nearly unchanged. Similarly, the increase in τ_{int} with T_{base} is primarily driven by the reduction in g_{m} at $(V_{\mathrm{GS}}, V_{\mathrm{DS}}) = (-1.5, 20)\,\mathrm{V}$. By contrast, at $(V_{\mathrm{GS}}, V_{\mathrm{DS}}) = (-2.5, 30)\,\mathrm{V}$, the degradation in τ_{int} results from the combined effect of decreasing g_{m} and increasing $C_{\mathrm{gs}}^{\mathrm{int}}$ (see Fig. 8(d)), leading to the most pronounced performance degradation among all delay components. At this quiescent point, $C_{\mathrm{gs}}^{\mathrm{int}}$ increases with temperature due to enhanced charge injection from the source contact into the channel, combined with the negative temperature coefficient of the threshold voltage. As T_{base} increases, this threshold-voltage shift effectively changes the gate-bias condition from slightly below threshold to right at threshold.

The temperature-dependent cutoff frequency estimated from the delay model is compared with the f_{T} values extracted from S-parameter simulations of the calibrated HEMT performed in Keysight ADS [34]. As shown in Fig. 9, the reduced-order delay model systematically overpredicts the absolute f_{T} obtained from the calibrated MVSG-RF model, with the largest discrepancy occurring near threshold. At the lower-V_{GS} bias, the relative discrepancy in f_{T} (delay) decreases from approximately +28% (22%) at 298 K to approximately +19% (16%) at 398 K. As the device is driven further into the on-state, the discrepancy is substantially smaller, decreasing from approximately 6% to 3% over the same temperature range. Importantly, the discrepancy does not increase with baseplate temperature at either bias condition. Thus, the principal limitation of the reduced-order delay model is a bias-dependent offset in the absolute value of f_{T}, particularly near threshold, rather than an increasing temperature-dependent error. Accordingly, the delay model is used here primarily to quantify the relative contributions of intrinsic, extrinsic, and parasitic delays and their evolution with bias and temperature, rather than as a replacement for the calibrated MVSG-RF model for precision prediction of the absolute cutoff frequency. It can be seen from this figure that for both quiescent operating points, f_{T} decreases by more than 20% when T_{base} is increased by $100\,\mathrm{K}$ from room temperature. The normalized f_{T} degradation rate of $0.2\%/\mathrm{K}$ is substantial and highlights the importance of incorporating temperature-dependent small-signal parameters when evaluating GaN HEMTs for thermally stressed power amplifier operation. The observed degradation rate of f_{T} is similar in magnitude to the experimental results demonstrated in [35] and [36] while more severe than the reported $0.1\%/\mathrm{K}$ over $233-423\,\mathrm{K}$ in [37] and $0.125\%/\mathrm{K}$ over $150 - 300\,\mathrm{K}$ range in [38]. These differences are expected as the magnitude of f_{T} degradation depends strongly on gate length, access resistance, buffer design, self-heating and bias conditions. Additional details of high-temperature DC calibration and the trends of small-signal parameters with temperature can be referred to in Supplementary Material Sec. II.

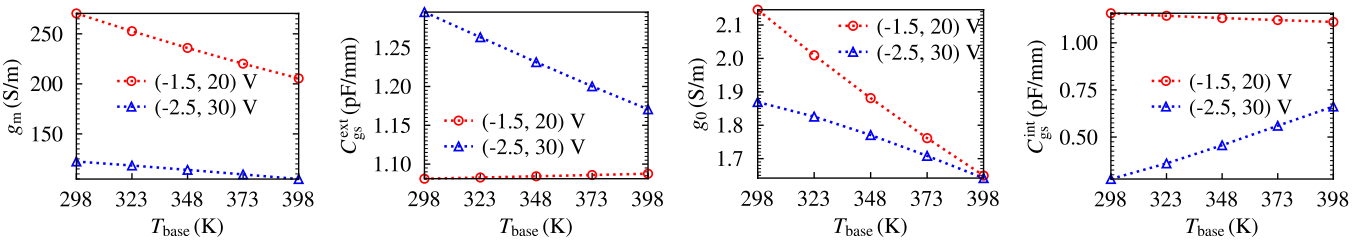
The decrease in f_{T} with increasing T_{base} has direct implications for GHz-range power amplifier operation. Since f_{T} represents the intrinsic current-gain bandwidth of the transistor, its reduction at elevated temperature lowers the available RF gain margin and can compromise high-frequency performance under high-power operating conditions.

We note that trap dynamics and the associated g_{m}/g_0 dispersion effects on f_{T} under varying T_{base} are not included in the GHz-frequency small-signal response. This omission may lead to a slight underestimation of current collapse; however, it does not affect our conclusions on the temperature dependence of f_{T}. In our samples, the Fe-related trap exhibits emission time constants on the order of 10^{-6} to $10^{-2}\,\mathrm{s}$ as T_{base} varies from 298 K to 413 K [11], which are substantially longer than the RF periods considered here; quasi-static trap effects are implicitly reflected in the measured characteristics used for model calibration.

IV. Conclusion

In summary, the calibrated MVSG-RF 1.1.0 compact model enables design-space exploration of the small-signal performance of a 0.5-μm fabricated AlGaN/GaN HEMT, with support from TCAD simulations and the analytical delay model. Using this framework, we evaluated the impact of elevated baseplate temperature and access-region scaling on f_{T}.

Elevated T_{base} degrades f_{T} primarily through the reduction of g_{m}, which increases both τ_{ext} and τ_{int}. Near-threshold biasing introduces an additional sensitivity: temperature-induced changes in threshold voltage



(a) g_{m} versus T_{base}. (b) $C_{\mathrm{gs}}^{\mathrm{ext}}$ versus T_{base}. (c) g_0 versus T_{base}. (d) $C_{\mathrm{gs}}^{\mathrm{int}}$ versus T_{base}.

Fig. 8. Extracted small-signal parameters at various baseplate temperatures.

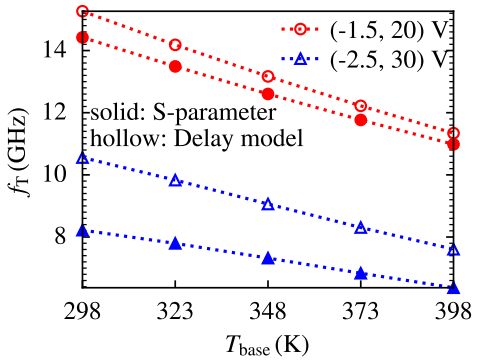


Fig. 9. Cutoff frequency vs. baseplate temperature formulated using both S-parameter directly from MVSG and using the simplified delay model. Symbols represent different $(V_{\mathrm{GS}}, V_{\mathrm{DS}})$ bias choices.

and channel charge modify $C_{\mathrm{gs}}^{\mathrm{int}}$, further amplifying the increase in τ_{int}. This makes the intrinsic delay the dominant pathway through which elevated temperature degrades f_{T}. The cutoff frequency is found to degrade at approximately $0.2\%/\mathrm{K}$, which is comparable to, and slightly higher than, prior reports, indicating that even moderate thermal loading can produce measurable degradation in high-frequency performance.

The parasitic delay, due to the source and drain access region resistances, contributes less than 13% of the total delay over the investigated temperature range. Thus, access-region scaling alone is insufficient for substantial improvement in RF performance. Although the present results indicate that reducing the access-region length provides only a modest improvement in g_{m} and f_{T} for this technology, this should not be interpreted as implying that access-region engineering is unimportant. In particular, the gate-to-drain spacing L_{gd} influences the peak drain-side electric field and therefore the breakdown voltage of GaN HEMTs [39]–[41]. Consequently, access-region design represents a tradeoff between minimizing access resistance/parasitic delay and maintaining adequate high-field robustness. This tradeoff may become increasingly important at elevated temperature, where thermally activated leakage and defect-assisted conduction can affect breakdown characteristics [42], [43]. Breakdown was not characterized in the present devices and is therefore beyond the scope of the current analysis. Additional comments on breakdown can be seen in Supplementary Material Sec. V.

More aggressive gains require direct scaling of the intrinsic gated channel while maintaining electrostatic integrity. Future work will extend this framework to assess the impact of channel-length scaling and elevated T_{base} on large-signal metrics of a GaN power amplifier.

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