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Abstract

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Mitsubishi Electric Research Laboratories, Inc.
201 Broadway, Cambridge, Massachusetts 02139

An accurate electrical and thermal co-simulation framework for modeling high-temperature DC and pulsed I-V characteristics of GaN HEMTs

Yicong Dong, Eiji Yagyu, Takashi Matsuda, Koon Hoo Teo, *Member, IEEE*, Chungwei Lin, Shaloo Rakheja, *Senior Member, IEEE*

***Abstract*—High-electron mobility transistors (HEMTs) employing AlGaN/GaN heterostructures are suitable for high-power and high-frequency applications. To meet target specifications, GaN HEMTs must be designed and optimized by accurately considering the coupling of electrical and thermal characteristics, from the static to the pulsed regimes of operation. Toward this, we implement an electro-thermal modeling and simulation framework for experimentally fabricated GaN on SiC HEMTs and use the framework to predict the high-temperature performance of the technology, up to 448 K. We utilize the transient measurement data at different ambient temperatures to extract the trap characteristics, which are important to understand from the RF dispersion perspective. Our work highlights the significance of the thermal boundary conditions at the source, drain, and gate metal electrodes and the impact of heat dissipation paths on the lattice temperature rise and I-V characteristics. Overall, our work provides a physical insight into the thermal response of GaN HEMTs and can facilitate suitable thermal management strategies of the device over a broad range of DC and transient operating conditions.**

***Index Terms*—Gallium nitride, HEMTs, thermodynamic transport, TCAD simulations, drain-current transients**

I. Introduction

GALLIUM nitride (GaN) is a wide-bandgap semiconductor material that is very well-suited for high-frequency and high-power applications [1]. Supported by their spontaneous and piezoelectric strains, AlGaN/GaN high-electron mobility transistors (HEMTs) feature a high concentration of the two-dimensional electron gas (2DEG) in the GaN channel [2]. The 2DEG's room-temperature mobility up to $1500\ \mathrm{cm^2/V.s}$ [3] and its saturation velocity close to $2 \times 10^7\ \mathrm{cm/s}$ [4] can enable the GaN HEMT to perform at high frequencies that are desirable for microwave and millimeter wave applications [5]. Moreover, the inherent wide bandgap near 3.4 eV [6] provides a superior breakdown voltage [7], one to two orders of magnitude larger than conventional alternatives such as gallium arsenide (GaAs) or silicon (Si) [8]. Last, but not least, thermal conductivity advantage of GaN [9] allows for more reliable operation under high temperature conditions than previous generation of semiconductors like Si and GaAs [10].

Significant experimental and theoretical efforts have been devoted to understanding the temperature-dependent thermal conductivity of GaN, both in the cryogenic limit and at temperatures far above the room temperature [9], [11]. The impact of structural design, for example, the number of fingers in the HEMT, is yet another focus of research on heat dissipation for such devices [12]. In both experiments and simulations, thermal boundary conditions are also extensively studied for the baseplate beneath the substrate, the side walls, and the interface between substrate and GaN epilayers [13]–[17], whereas top of the wafer is almost always treated as adiabatic. Despite the significant research progress, challenges remain in understanding the role of thermal boundary conditions and the various heat dissipation pathways on the device's electro-thermal response under various applied biases. Moreover, the calibration of device models with experimental measurements can be quite cumbersome and yield unphysical model parameters if the physics of self-heating is not accurately represented.

In this paper, we implement an electro-thermal co-simulation framework of AlGaN/GaN on SiC HEMTs that were fabricated at Mitsubishi and characterized for their DC and transient behavior over a broad temperature range, from 298 K to 448 K. The electrical transport

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Y. Dong (e-mail: yicongd2@illinois.edu) and S. Rakheja (e-mail: rakheja@illinois.edu) are with the Holonyak Micro and Nanotechnology Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801.

E. Yagyu (e-mail: Yagyu.Eiji@cb.MitsubishiElectric.co.jp) and T. Matsuda (e-mail: Matsuda.Takashi@dn.MitsubishiElectric.co.jp) are with the Mitsubishi Electric Corporation, Amagasaki 661-8661, Japan

K. H. Teo (e-mail: teo@merl.com) and C. Lin (e-mail: clin@merl.com) are with the Mitsubishi Electric Research Laboratories, Cambridge, MA 02139.

is modeled using the drift-diffusion theory, while the heat flow in the device is captured using the Fourier's heat equation. Our models investigate the impact of thermal resistance at the top electrodes on the device lattice heating and the resulting current flow, as well as drain current transient (DCT) response of the device. Specifically, we vary the surface thermal conductance of the top electrodes from zero to very large values, such that the thermal boundaries are one of adiabatic (Neumann insulating), non-homogeneous Neumann, or close to Dirichlet. We calibrate the TCAD models against measurement data and highlight physics pertinent to lattice heating, trap characteristics, and device reliability. Our work provides suggestions to the community with regards to a more accurate and efficient TCAD modeling of AlGaN/GaN HEMTs.

II. Method

A. Device Structure

The structure of the device under test (DUT) is shown in Fig. 1. In this structure, GaN epilayers are grown on top of the SiC substrate, while $Al_{0.23}Ga_{0.77}N$ on top of the GaN channel serves as an insulating barrier. A GaN cap of $2\ \mathrm{nm}$ is above the insulator, and the mushroom gate is made of Ni, and a Schottky barrier height of $1.25\ \mathrm{eV}$ at the gate-GaN cap metal-semiconductor (MS) junction [18] is assumed, while titanium/niobium (Ti/Nb) drain and source contacts are assumed to be ohmic and heavily doped underneath.

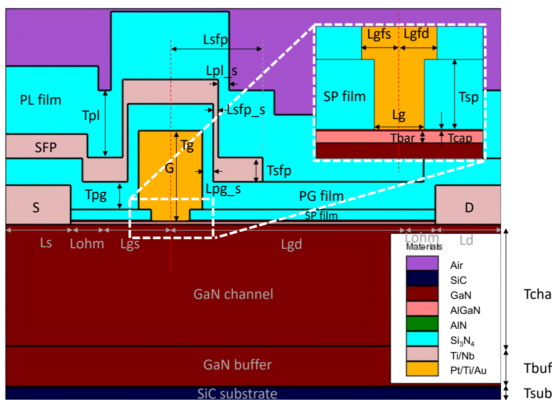

Fig. 1. Cross-section of the fabricated AlGaN/GaN HEMT with labeled materials and dimensions (see Table I). Inset is a closer view at the alloy gate/GaN cap/barrier/GaN channel structure.

Relevant dimensions of the DUT have been labeled in Fig. 1 and denoted in Table I, including but not limited to the electrode lengths, channel length, access regions lengths, thickness of different layers, and additional components such as field plates and silicon nitride (Si_3N_4) passivation (SP) film. Not shown is the width of the gate (W), which is different for static and transient measurements since multiple samples were fabricated.

TABLE I
Geometric dimensions of the fabricated AlGaN/GaN HEMT corresponding to labels in Fig. 1.

Thickness	Dimension (μm)	Length	Dimension (μm)
Tsub	0.5	Lg	0.5
Tcha	0.9	Ls	1
TbufSi	0.1	Ld	1
Tbuf	0.3	Lgs	1
Tbuf2	0.007	Lgd	3.5
Tcap	0.002	Lohm	0.5
Tbar	0.02	Lgfs	0.5
Tsp	0.09	Lgfd	0.5
Tpg	0.2	Lsfp	1
Tpl	1	Lpg_s	0.2
Tg	0.6	Lsfp_s	0.08
Tsfp	0.2	Lpl_s	0.2

For fair comparison, we always report quantities such as current and power normalized to the device width. The dimensions are rounded to the nearest single significant digit or nearest $0.5\ \mu\mathrm{m}$ for the fabricated devices because further details of Mitsubishi's technology cannot be disclosed.

The fabrication process for the AlGaN/GaN HEMT DUT involves several key steps. Initially, the GaN epilayers are grown on a SiC substrate using metal-organic chemical vapor deposition (MOCVD). Isolation is achieved through Ar implantation. For the ohmic drain/source contacts, Si implantation is followed by activation annealing. Subsequently, electron beam evaporation of a titanium/niobium (Ti/Nb) is performed, followed by rapid thermal annealing. These contacts are defined using conventional photolithography and lift-off techniques. The gate contact, on the other hand, involves platinum (Pt) sputtering followed by titanium/platinum/gold (Ti/Pt/Au) evaporation, also defined by conventional photolithography and lift-off techniques and with titanium (Ti) deposited first in the second deposition to enhance adhesion to the initial Pt layer. Finally, the device is passivated using CVD of Si_3N_4 to enhance performance and reliability.

For electrical measurements and modeling, the source, baseplate, and the source field plate (SFP) electrodes are grounded, while a bias is applied at gate (V_g) and drain (V_d), and the current, I_d, entering the drain terminal is measured. $I_\mathrm{d} = I_\mathrm{ds} + I_\mathrm{gs}$, where I_ds is the drain current that flows toward the source, while I_gs is the drain current that flows toward the gate.

For 2-D TCAD simulation purposes through the finite element method, we discretize the structure into triangular elements as shown in Fig. 2. The mesh grids are adaptive, specifically finer near the top of the channel, interface between channel and buffer, interface between buffer and substrate, and interface between Si_3N_4 and GaN cap. This ensures that simulation of transport is

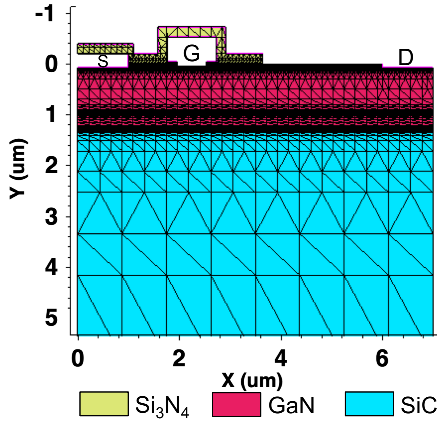

Fig. 2. TCAD finite element mesh of the fabricated AlGaN/GaN HEMT. Colors are for different materials, and the view is truncated to show only part of the SiC substrate.

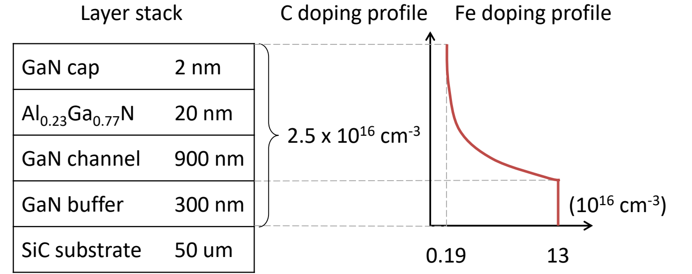

Fig. 3. Doping profile of carbon and iron in the fabricated AlGaN/GaN stack.

well-captured while simulation of lattice temperature is not sacrificed with decreased simulation time and computational expense. Note that not all regions of the Si_3N_4 films are simulated. SP film as well as Passivation Gate (PG) film up to regions covered by the SFP are simulated while any other nitride above SFP or drain electrode are not simulated as also shown in Fig. 2.

B. Compensation Doping and Poisson's Equation

The intentional acceptor-type doping of the DUT is shown in Fig. 3. In addition, we assume that the sample contains a donor-type unintentional dopant (UID) located $50\ \mathrm{meV}$ below the conduction band minimum of GaN. The UID is attributed to oxygen and Si atoms introduced in GaN during the MOCVD growth [19]. The density of the UID (N_{UID}) is treated as a fitting parameter in simulation to achieve compensation doping of the buffer in order to reduce buffer leakage. The intentional acceptors are carbon (C) with an energy level $0.9\ \mathrm{eV}$ above the valance band maximum (E_{V}) [20] and iron (Fe) with an energy level $0.5\ \mathrm{eV}$ below the conduction band minimum (E_{C}) [21]. C-doping is uniform, while Fe-doping is Gaussian as shown in Fig. 3. Carbon enables compensation doping of the buffer as it is located below the mid-gap. However, the activation energy of de-trapping of electrons from carbon is rather high. On the other hand, iron doping can minimize drain lag as its energy level is closer to the conduction band and can thus enable fast de-trapping of electrons and thus a fast recovery of transient drain current.

To understand the compensation doping scheme in our DUT, let us consider the Poisson equation:

$$-\frac{\nabla\cdot(\epsilon_{\mathrm{r}}\epsilon_0\nabla\phi)}{q}=p-n+N_{\mathrm{UID}}^{+}-N_{\mathrm{iron}}^{-}-N_{\mathrm{carbon}}^{-}, \quad (1)$$

where q is the unit charge, ϵ_{r} is the relative permittivity (8.9 for GaN and AlGaN [22]), ϵ_0 is the vacuum permittivity, ϕ is the electrostatic potential, p is the hole density, n is the electron density, N_{UID}^{+} is the positively ionized UID density, while N_{iron}^{-} and N_{carbon}^{-} are the negatively ionized iron and carbon densities, respectively. The densities of various species are calculated using Fermi-Dirac statistics, and we set $N_{\mathrm{V}}=4.62\times10^{19}\ \mathrm{cm}^{-3}$ and $N_{\mathrm{C}}=2.23\times10^{18}\ \mathrm{cm}^{-3}$ for the effective density of states for the valence band and conduction band, respectively, in GaN [22]. For all TCAD simulations, the intrinsic energy E_{i} is selected as reference energy, and the trap activation energy (E_{a}) is always defined relative to the conduction or valance band edges. As mentioned previously, the energy level of UID, $E_{\mathrm{UID}}=50\ \mathrm{meV}$ below the conduction band edge in GaN, while the UID density, N_{UID}, is an unknown parameter that is extracted to yield a good fit of the model-generated sub-threshold characteristics against the measurement data (see Sec. III-B for the optimal fit). According to Fig. 4, if N_{UID} is too large, the DUT never turns off, whereas if N_{UID} is too small, the sub-threshold swing is underestimated over four different V_{d}'s. For $N_{\mathrm{UID}}\approx3\times10^{16}\ \mathrm{cm}^{-3}$, our estimated buffer equilibrium Fermi energy is $E_{\mathrm{F}}=0.58\ \mathrm{eV}$ below E_{C}, and the resistivity is $3.7\times10^{8}\ \Omega.\mathrm{cm}$ favoring 2DEG confinement to prevent substrate leakage current. On the other hand, the surface of the GaN channel region has $E_{\mathrm{F}}=0.17\ \mathrm{eV}$ below E_{C}, and the resistivity is $1.72\ \Omega.\mathrm{cm}$, which in contrast largely favors electron conduction.

C. Coupled carrier transport and heat flow

To study carrier transport in the presence of self-heating, current continuity equations with drift-diffusion transport models and Fourier's heat law that accounts for lattice temperature distribution are solved self-consistently, where we consider lattice heat capacity c_{L} to be $2.16\ \mathrm{J/K.cm^3}$ for SiC and $2.6\ \mathrm{J/K.cm^3}$ for GaN [22]. Thermal conductivity κ for GaN and SiC is further discussed in Sec. II-E. Although the GaN HEMT is a majority carrier (*i.e.*, electron) device, we solve for both electrons and holes to faithfully capture the physics

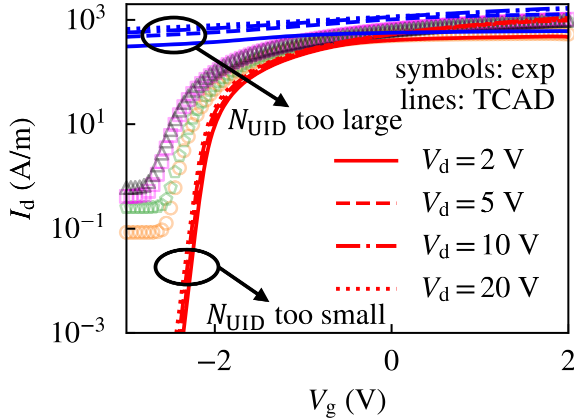

Fig. 4. Impact of UID concentration on the off-state characteristics for different drain bias values.

of compensation doping and present a more holistic picture of the transport over a broad bias and temperature regime. As a result of majority carrier transport, SRH recombination is negligible in our calculations. The hole mobility, μ_p, is assumed to be constant at $150\ \mathrm{cm^2/V.s}$ for GaN – its impact on transport calculations is insignificant as the current conduction through the channel is due to electrons. The electron mobility, μ_n, in GaN is dependent both on the magnitude of the driving force (F_{hfs}) interpolated between electric field and gradient of quasi-Fermi energy and on the lattice temperature (T), and it follows the Canali mobility model [23] as

$$\mu\left(F_{hfs},T\right)=\frac{\mu_{low}\left(\frac{T}{300\ \mathrm{K}}\right)^{-\epsilon}}{\left[1+\left(\frac{\mu_{low}F_{hfs}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}}, \quad (2)$$

where μ_{low} is the low field mobility, v_{sat} is the saturation velocity, β is an empirical parameter describing the linear to saturation transition of the output current, and ϵ is an empirical parameter describing mobility degradation due to lattice temperature rise. For our DUT, β is found to depend on T according to

$$\beta=\beta_0\left(\frac{T}{300\ \mathrm{K}}\right)^{\beta_{exp}}, \quad (3)$$

where β_0 is the pre-factor, while its temperature dependence is of a power-law form with β_{exp} representing the temperature coefficient. The electron (hole) mobility in AlGaN is assumed to be $300\ \mathrm{cm^2/V.s}$ ($50\ \mathrm{cm^2/V.s}$), constant at all temperatures [24]. SiC substrate is treated as an electrical insulator for simplicity.

The saturation velocity, v_{sat}, is found to depend on V_g for $V_g > 0$ due to an increase in the longitudinal optical (LO) phonon emission. More specifically, drift velocity saturates in GaN when the phonon gain, which occurs when the probability of stimulated LO phonon emission exceeds the probability of LO phonon absorption, reaches a carrier concentration dependent threshold value [25]. Previous work has shown that the saturation velocity in GaN varies as $n_{2DEG}^{-1/m}$, where $m \in [2,4]$ depends on the detailed physics [26]. In our work, we make v_{sat} dependent on V_g, as the n_{2DEG} in the channel is controlled by V_g and thus our model can capture the desired physics. See Sec. III-B for additional details regarding the extraction of $v_{sat}(V_g)$ for our DUT.

D. Forward Gate Leakage

Aside from possible current leakage from the channel into the buffer, gate leakage is yet another component that must be included in the model. Depending on the relative magnitude of V_g and V_d, gate leakage can happen through different mechanisms. For $V_g < 0$, reverse leakage occurs mainly through Fowler–Nordheim tunneling [27], Poole–Frenkel emission [28] and trap-assisted tunneling [29]. For $V_g > 0$ and $V_g > V_d$, thermionic emission is more likely the dominant term [30]. In this work, we consider only forward gate leakage through thermionic emission (see Fig. 5) since we are more interested in the on-state of the device for switching dynamics and thermal reliability under heating.

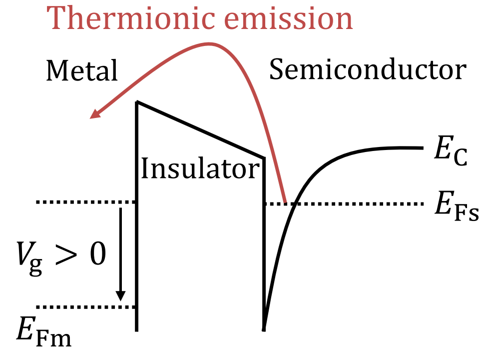

Fig. 5. Forward gate leakage through thermionic emission. E_{Fm} and E_{Fs} are the quasi-Fermi levels of the gate metal and the semiconductor, respectively.

The thermionic current at a heterojunction of materials i and j is given as

$$J_{n,ij}=2q\left[v_{n,i}n_i-\frac{m_{n,i}}{m_{n,j}}v_{n,j}n_j\exp\left(-\frac{\Delta E_C}{k_BT_{n,j}}\right)\right], \quad (4)$$

where $k_BT_{n,j}$ is the thermal energy of material j, $J_{n,ij}$ is the electron current density leaving material j and entering material i, $v_{n,i}=\sqrt{\frac{k_BT_{n,i}}{2\pi m_{n,i}}}$ is the electron emission velocity in material i, n_i is the electron density in material i, and $m_{n,i}$ is the electron effective mass in material i. In Sec. III-B, we show that drain current of the device is negative current for $V_g = 2$ V near $V_d = 0$ V, and the calibration of this regime requires that thermionic

emission is included in the model to allow electron transport from GaN channel to the gate electrode through the AlGaN insulator, *i.e.*, current flow from gate to drain. With this current component, $I_{\rm gd} > 0$ and $I_{\rm ds} \approx 0$, it would then make sense that $I_{\rm d} = I_{\rm ds} + I_{\rm dg} < 0$.

E. Thermal Boundary Condition

It is critical to consider the thermal boundary conditions of the HEMT structure to converge to a physical solution corresponding to the self-consistent electro-thermal dynamics. Conventionally, the baseplate is set to be a Dirichlet thermal boundary with a fixed temperature, while the drain/source/gate metal electrodes have the Neumann boundary condition with zero heat flux leaving the surface. This implies that the metal electrodes are adiabatic or thermally insulating in nature. However, thermally insulating top metal electrodes lead to an overestimation of thermal resistance of the DUT and thus unreasonably hot lattice temperatures almost 400 K higher than the ambient (baseplate). As shown in Fig. 6, despite adjusting the thermal conductivity of SiC and GaN, while keeping metal electrodes as thermally insulating, the model-generated output curves at high output power levels display a much more significant negative differential conductance compared to experimental data. The severe negative differential conductance implies an overestimation of the self-heating and is indicative that the thermal boundary condition wherein the top electrodes are treated as adiabatic is inadequate to describe the electro-thermal response of the DUT.

To accurately capture the thermal behavior of the DUT, we consider a non-homogeneous Neumann boundary condition at each of the top electrodes, which is specified as

$$\kappa_{\rm GaN}\hat{n} \cdot \nabla T = \frac{T_{\rm ext} - T}{R^i_{\rm th}}, \tag{5}$$

where $\hat{n}$ is the direction normal to an electrode, $T_{\rm ext}$ is the ambient (probe) temperature (considered independent of the thermal resistance), and $R^i_{\rm th}$ is the surface thermal resistance of the electrode, i corresponds to either source/drain/SFP (ds) or gate (g). Note that $R^i_{\rm th} = 0$ is equivalent to Dirichlet boundary condition, and $R^i_{\rm th} = \infty$ is equivalent to Neumann boundary condition. In our simulations, $T_{\rm ext}$ is set to be same as $T_{\rm base}$, presuming that the probes have the same temperature as the baseplate due to long time elapse before device characterization is conducted after turning on the baseplate heat source. Results showing output characteristics with different thermal conductances, $K^{\rm ds}_{\rm th} = \frac{1}{R^{\rm ds}_{\rm th}}$, ranging from 10^3 W/cm^2.K to 10^5 W/cm^2.K are presented in Fig. 7. The gate electrode is assumed to have twice the

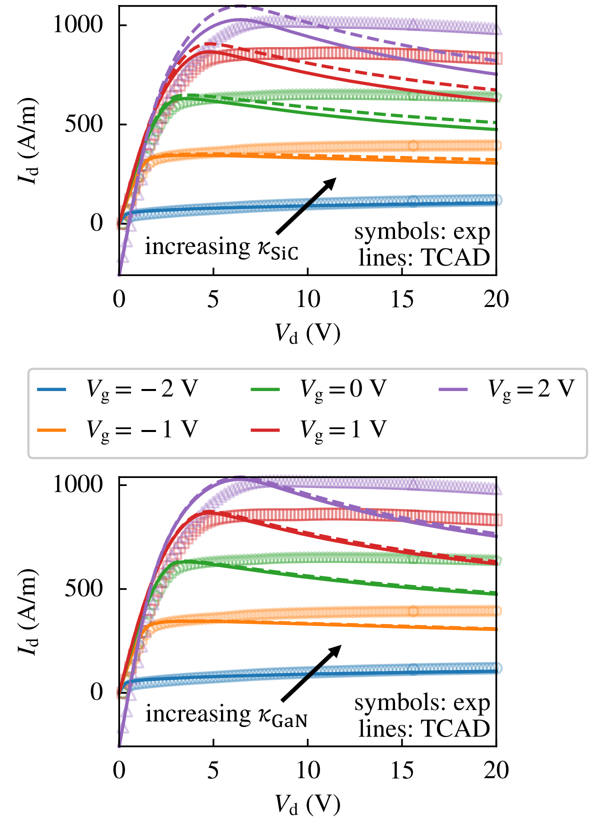

Fig. 6. Impact of (top) SiC and (bottom) GaN thermal conductivity on output characteristics at $T_{\rm base}$ = 298 K with adiabatic drain/source thermal boundary conditions. (top) Solid lines: $\kappa_{\rm SiC}$ = 350 W/m.K, dashed lines: $\kappa_{\rm SiC}$ = 450 W/m.K [9]. (bottom) Solid lines: $\kappa_{\rm GaN}$ = 130 W/m.K, dashed lines: $\kappa_{\rm GaN}$ = 210 W/m.K [31].

surface thermal conductance of that of the source/drain electrodes. As the values of $K^{\rm ds}_{\rm th}$ and $K^{\rm g}_{\rm th}$ increase, the equivalent total thermal resistance of our DUT decreases due to better heat dissipation near the contact boundaries. As a result, the differential output conductance becomes less negative when the total DUT thermal resistance reduces. Thus, the surface thermal conductance of the electrodes must be tuned to yield an optimal matching of the model-generated results with measurement data in the saturation regime. Assuming Ti/Nb (gate) thermal conductivity of 150 W/m.K [32]–[35] and that of Nb/Pt/Au (source/drain) of 35 W/m.K [36], we find $K^{\rm g}_{\rm th} = 2.5 \times 10^4$ W/cm^2.K and $K^{\rm ds}_{\rm th} = 1.2 \times 10^4$ W/cm^2.K. Thus, $K^{\rm g}_{\rm th}$ is found to be twice as high as $K^{\rm ds}_{\rm th}$. For the purposes of model calibration, we have chosen to fix $K^{\rm g}_{\rm th}/K^{\rm ds}_{\rm th} = 2$, while varying the value of $K^{\rm ds}_{\rm th}$.

Inspecting the lattice temperature heatmaps in Fig. 8 and comparing with negative differential current in the saturation regime shown in Fig. 7, we conclude that $K^{\rm ds}_{\rm th}$ on the order of 10^3 W/cm^2.K results in heat flow towards both the bottom of the device and the

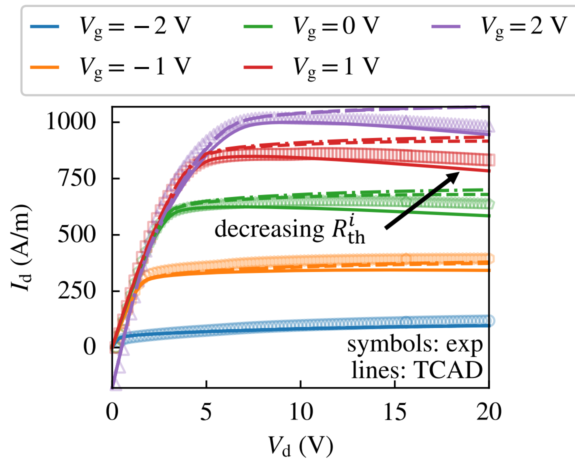

Fig. 7. Impact of electrode surface thermal conductance on output characteristics at $T_{\mathrm{base}} = 298$ K with $\kappa_{\mathrm{SiC}} = 350$ W/m.K and $\kappa_{\mathrm{GaN}} = 130$ W/m.K. Line styles from top to bottom are for drain/source surface thermal conductances of $\{10^5, 10^4, 10^3\}$ W/cm^2.K. Gate surface thermal conductance is set to be twice that of drain/source values.

top contacts. Further, we provide supplementary evidence that the maximum lattice temperature varies with different $K^{\mathrm{ds}}_{\mathrm{th}}$ as shown in Fig. 9. The temperature is vastly overestimated for a small choice of $K^{\mathrm{ds}}_{\mathrm{th}}$ upto around 600 K, while on the other hand, temperature rise becomes negligible for a very large choice such as $K^{\mathrm{ds}}_{\mathrm{th}} = 10^5$ W/cm^2.K, the heat dissipation from the top contacts is rather too high to be physically plausible, and for this boundary condition, the heat dissipates primarily through the top contacts, thus underestimating the DUT thermal resistance. Only for the selected boundary condition ($K^{\mathrm{ds}}_{\mathrm{th}} = 1.4 \times 10^3$ W/cm^2.K), the model-generated output characteristics exhibit thermal resistance, *i.e.*, negative differential conductivity very close to that of our DUT. To summarize, the heat generated in the device flows through multiple paths and it is thus insufficient to only focus on vertical heat conduction toward the base plate. In this regard, the model setup presented here, with appropriate thermal boundary conditions, offers a realistic picture of the device's electro-thermal behavior and can be used to study device reliability.

III. Results

A. Setup for Transfer, Output, and DCT

For thermal reliability studies, we focus on device measurements conducted up to 448 K. Starting with transfer characteristics, we have four distinct V_d's and sweep V_g from the off-regime to the on-regime for four different T_{base} values as summarized in Table II.

By calibrating the model-generated transfer curves against measurement data, we extract the values of three physical parameters in the model: $\sigma^{\mathrm{gate}}_{\mathrm{pol}}$, which

TABLE II
DC bias setup for transfer characteristics.

V_d (V)	V_g (V)	T_{base} (K)
2	$[-3, 2]$	298
5		323
10		373
20		423

corresponds to the polarization sheet charge density at the AlGaN barrier/GaN channel in the gated region, N_{UID}, which affects the sub-threshold swing particularly at high V_d values, in the off-state, and $\sigma^{\mathrm{acc}}_{\mathrm{pol}}$, which is the polarization sheet charge in the access regions. In particular, we tune $\left(\frac{\sigma^{\mathrm{acc}}_{\mathrm{pol}}}{\sigma^{\mathrm{gate}}_{\mathrm{pol}}}\right)$ for purposes of model calibration. The polarization charge factor dictates both the sub-threshold swing in the transfer characteristics and the linear regime slope and the saturation current in the output characteristics, and has separate values selected for drain and source access regions.

After calibrating the transfer characteristics, we calibrate the output characteristics for which we have five distinct V_g measurements, while V_d is swept from the linear to the saturation regime for three different T_{base} values as summarized in Table III.

TABLE III
DC bias setup for output characteristics.

V_d (V)	V_g (V)	T_{base} (K)
$[0, 20]$	-2	298
	-1	
	0	323
	1	373
	2	

From calibrating the model-generated output curves against measurement data, we can extract parameters corresponding to electron transport. For example, μ_{low} is obtained from the slope of the linear output curves, while v_{sat} can be determined from the saturation current value. In addition, the saturation current measured at different V_g values can be employed to extract β and source access region polarization sheet charge $\sigma^{\mathrm{source,acc}}_{\mathrm{pol}}$ as these parameters limit the ohmic sheet resistance of the channel. The thermal resistances of GaN and SiC are determined from Transfer Length Measurements [37] not presented in this paper, while the electrode thermal boundary conditions are adjusted to yield accurate negative differential resistance of the DUT under high power levels.

Using the TCAD model, we also calibrate key temporal attributes of the measured DCT data for T_{base} in the range of 298 K to 413 K. The transient pulse train profiles for V_g and V_d are illustrated in Fig. 10, where there is a 10 ms emission phase and a 90 ms

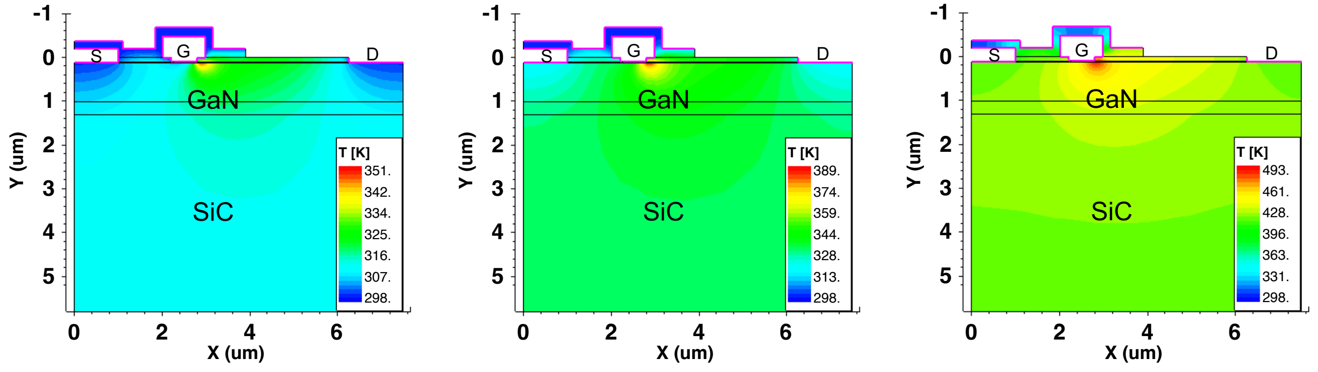

Fig. 8. TCAD simulated lattice temperature heatmap (truncated view) at $T_{\text{base}} = 298$ K, $V_{\text{g}} = 2$ V and $V_{\text{d}} = 20$ V for drain/source surface thermal conductance of (left) 10^5 W/cm.K, (middle) 10^4 W/cm.K and (right) 10^3 W/cm.K.

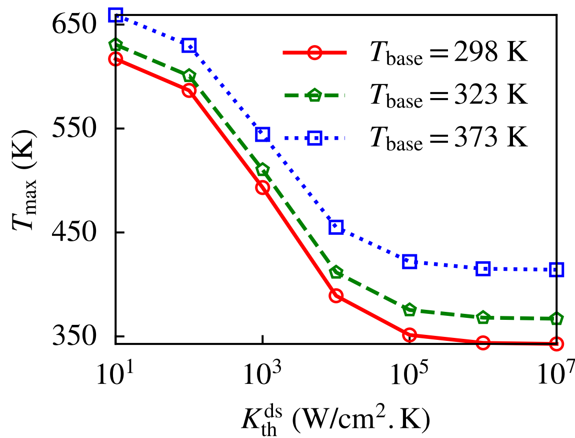

Fig. 9. Maximum lattice temperature vs. surface thermal conductance for various baseplate temperatures.

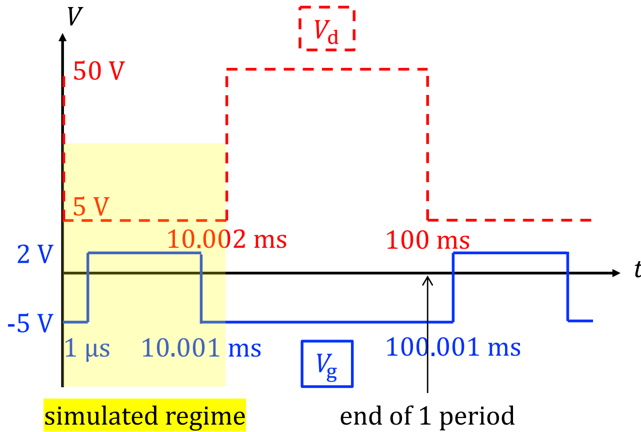

Fig. 10. DCT bias profile over time for both gate and drain. The emission phase lasts from 0 to 10 ms, followed by a recovery phase from 10 ms to 100 ms. Slopes of the voltage switching are not shown whose default value is 1 µs.

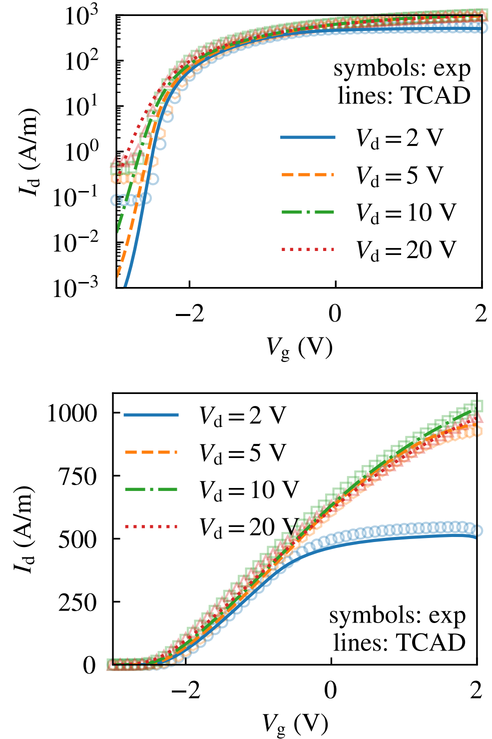

Fig. 11. TCAD and experiment transfer characteristics at $T_{\text{base}} =$ 298 K in (top row) logarithmic and (bottom row) linear scale.

recovery phase. At high V_{d} and low V_{g}, the DUT is off, and traps mostly capture electrons and have high occupation probability. At moderate V_{d} and high V_{g}, the DUT is on, and traps emit electrons back into the channel with the well-known drain-lag effect [38]. We focus on the emission phase to better understand trap signatures in the DUT using experimental results that average approximately 10 repetitions of measured drain output current. In TCAD, it is assumed that the recovery phase is steady-state, and transient simulation begins with the V_{d} switching at $t = 0$. The approximate switching time for both biases are about 1 µs, the slope of which is not shown on the vertical lines of Fig. 10 for better clarity of time delays between drain and gate switching.

B. Calibration of the model against DC measurements

1) Transfer Characteristics: Figure 11 shows the model-generated transfer curves overlaid on measurement data for room temperature. Fittings with experiments are achieved also for high temperatures but not

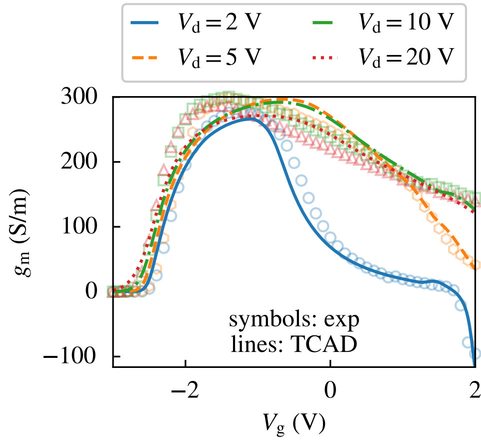

Fig. 12. TCAD and experiment transconductance at $T_{\text{base}} = 298$ K.

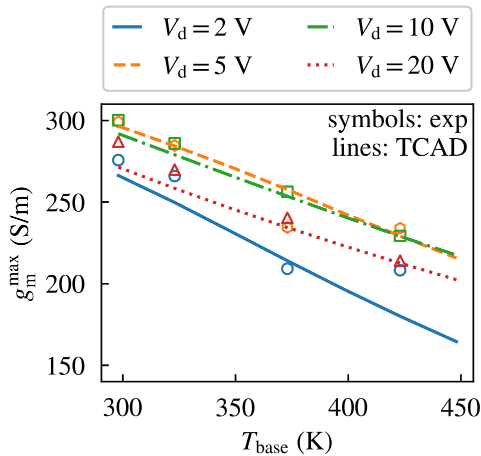

Fig. 13. TCAD and experiment maximum transconductance vs. baseplate temperature.

shown for simplicity. Our simulations faithfully capture the threshold voltage and sub-threshold swing of the DUT, although the gate leakage at large negative gate bias has not been included in our model.

The transconductance obtained from the model overlaid on measurement data is shown in Fig. 12. A summary of peak transconductance ($g_{\text{m}}^{\text{max}}$) is presented in Fig. 13, which shows a reasonably good fit with experimental data up to 423 K and can be further improved for small V_{d} values in future work. Thanks to the V_{g}-dependent saturation velocity, the non-linear transconductance degradation observed in experiments is correctly captured in TCAD. Our model validation shows that v_{sat} is constant for $V_{\text{g}} < 0$ V and linearly decreases for $V_{\text{g}} \geq 0$ V. This ensures that g_{m} decreases at high V_{g} values due to the stimulated emission of hot phonons at large 2DEG concentration. There is a very subtle change in the slope of g_{m} near $V_{\text{g}} = 0$ V for high V_{d} values due to the logistic function transition of v_{sat} in that region.

2) Output Characteristics: Figures 14 and 15 show the fit of the simulated output curves and the output conductance, respectively, against measurement data at room

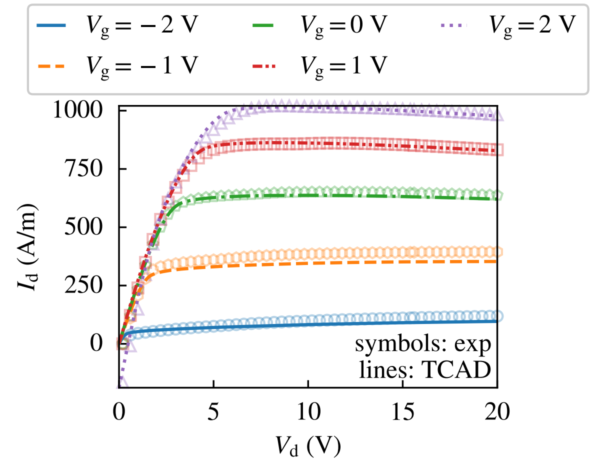

Fig. 14. TCAD and experiment output characteristics at $T_{\text{base}} = 298$ K.

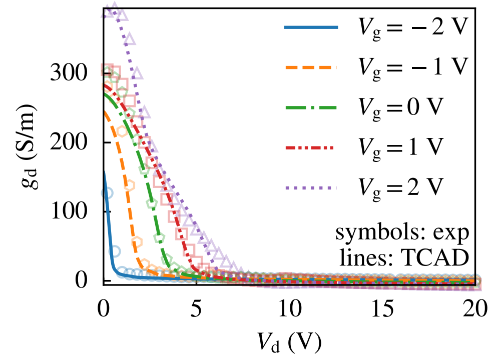

Fig. 15. TCAD and experiment output conductance at $T_{\text{base}} = 298$ K.

temperature. Fittings with experiments are achieved also for high temperatures but not shown for simplicity. Inclusion of forward gate leakage ensures that the negative I_{d} regime for $V_{\text{g}} = 2$ V is also well-captured. Overall, the model fits are robust and can be used to predict the device performance at higher temperatures for which measurement data is not available.

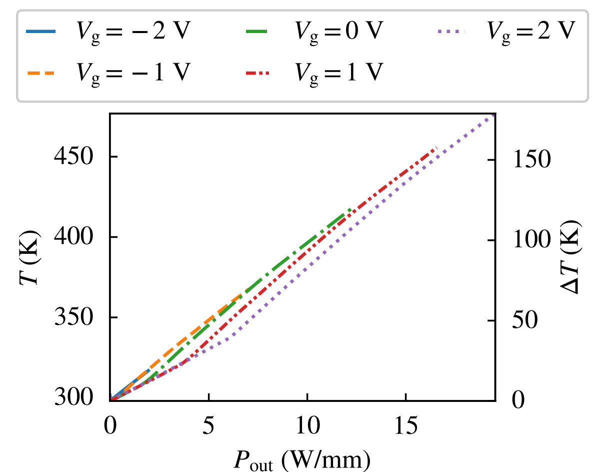

Fig. 16. TCAD simulated (left y-axis) maximum lattice temperature and (right y-axis) maximum temperature rise vs. output power at $T_{\text{base}} = 298$ K.

Using the calibrated model, we obtain the maximum lattice temperature of the DUT across different output power levels, as shown in Fig. 16. As expected, for a given output power level, the peak lattice temperature rises. Since the lattice temperature rise for a constant thermal resistance is given as $\Delta T = R_{\rm th}P_{\rm out}$, all curves at different $V_{\rm g}$ values but the same $P_{\rm out}$ fall on top of each other. The information on lattice heating is critical for estimating device reliability; however, measurements typically cannot probe the hottest temperature in a HEMT structure due to limited spatial resolution and slow read-out rate [39]–[41] and thus our model can be used for further reliability analysis.

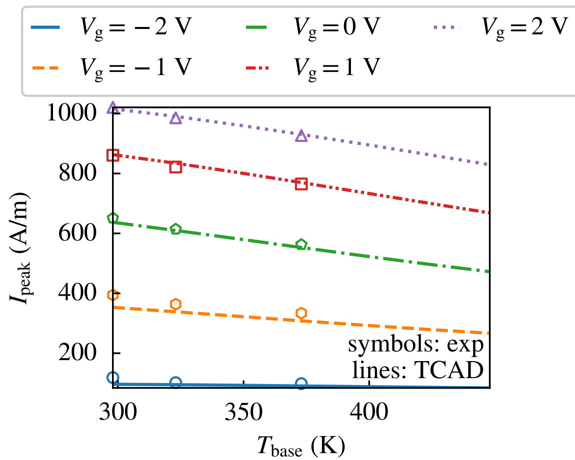

Fig. 17. TCAD and experiment peak output current vs. baseplate temperature.

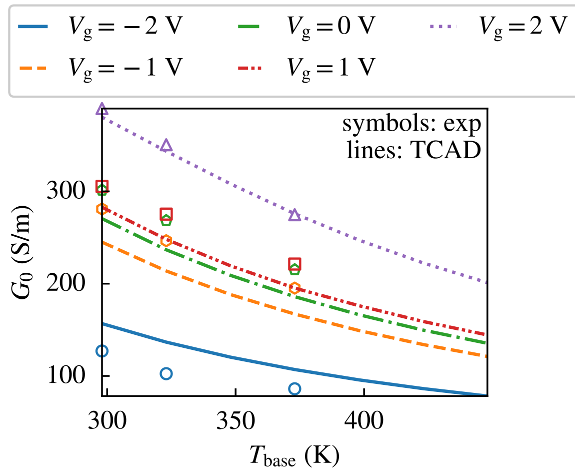

Fig. 18. TCAD and experiment linear output conductance vs. baseplate temperature.

We also summarize key performance metrics of the DUT at different $T_{\rm base}$ values in Figs. 17-19. Good agreement of peak current ($I_{\rm peak}$) and linear output conductance (G_0) is observed between TCAD and experiments, indicating that the linear regime and the transition from the linear to the saturation regime have been

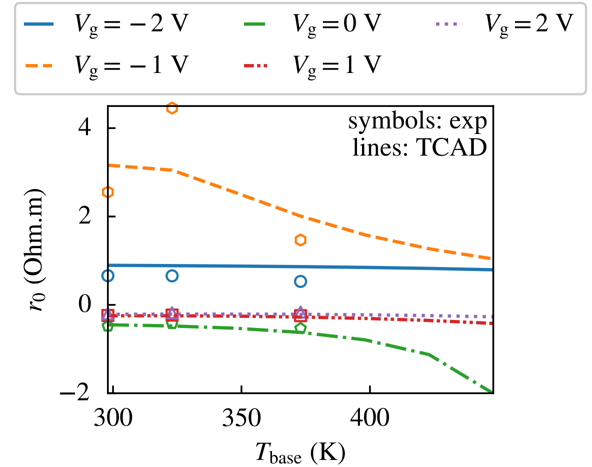

Fig. 19. TCAD and experiment saturation resistance vs. baseplate temperature.

calibrated. The saturation resistance (r_0) is imperfectly matched with experiments particularly for $V_{\rm g} = -1$ V as experiments show non-monotonic trend with increasing temperature, and the reason of this behavior is uncertain. Calibration of this performance metric will be cumbersome, and the exact trend is not easy to predict without further experimental evidence at this point.

C. Summary of model parameters

The parameters used in the DC model to yield a good fit with measurement data are reported in Table IV. Notably, the source and drain access regions have a higher sheet charge density than the gated region to ensure that the access region resistance is correctly interpreted by the model and that the model fits are accurate over a broad bias range. The surface thermal conductance of the electrodes is on the order of 10^3 W/cm^2.K, and a ratio of two is kept between the sd and g thermal conductances.

The extracted saturation velocity versus $V_{\rm g}$ is shown in Fig. 20. The maximum $v_{\rm sat}$ is $2.3{\times}10^7$ cm/s for negative gate voltages, and the lowest $v_{\rm sat}$ for the highest applied gate bias in our DUT is 1.5×10^7 cm/s. Five discrete $v_{\rm sat}$ values are used for output characteristics. A custom logistic function fitted to the discrete values serves the purpose of joining the constant regime and the linearly decreasing regime, and is incorporated into the transfer characteristics specifically to capture transconductance degradation.

D. Calibration of the model against transient measurements

1) Arrhenius Plot Construction: Preceding TCAD simulations of DCT, relevant trap-associated time constants are extracted from the DCT measurements at

TABLE IV
SUMMARY OF TCAD MODEL PARAMETERS.

Symbol	Explanation	Value
Φ_B	Schottky barrier	1.25 eV
σ_{pol}^{gate}	Gated region polarization charge	8×10^{12} cm^{-2}
σ_{pol}^{acc}	Access region polarization charge	Drain: $1.25\sigma_{pol}^{gate}$, source: $1.65\sigma_{pol}^{gate}$
N_{UID}	Unintentional shallow donor concentration	3.5×10^{16} cm^{-3}
E_{iron}	Iron acceptor energy	$E_C - 0.5$ eV
E_{carbon}	Carbon acceptor energy	$E_V + 0.9$ eV
κ_{GaN}	Thermal conductivity of GaN thin film	130 W/K.m
κ_{SiC}	Thermal conductivity of SiC substrate	350 W/K.m
K_{th}^{ds}	Surface thermal conductance of drain/source/SFP	1.4×10^3 W/cm^2.K
K_{th}^{ds}	Surface thermal conductance of gate	2.8×10^3 W/cm^2.K
μ_n^{low}	Low-field bulk electron mobility at 300 K	1400 cm^2/V.s
ϵ	Temperature-dependent mobility	2.2
v_{sat}	Saturation velocity	Refer to Fig. 20
β_0	Linear to saturation transition empirical parameter	1.4
β_{exp}	Temperature-dependent β parameter	1.5

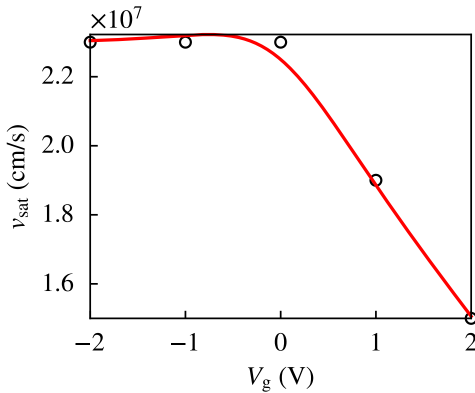

Fig. 20. Extracted V_g-dependent v_{sat} for our DUT. Black circles are discrete optimal v_{sat} choices for output characteristics, and red line is an artificial logistic function fitted to the observed v_{sat} and adopted for transfer characteristics as well as capturing transconductance degradation.

different T_{base} values. We assume that the DCT data can be represented as [42]

$$I(t) = A_0 - \sum_{i=1}^{N} A_i \exp\left(-\frac{t}{\tau_i}\right), \qquad (6)$$

where A_0 is the DC amplitude, A_i is the transient amplitude of the i-th trap, τ_i is the i-th trap's time constant constant, and N is the number of time constants (or traps) present in the data. From fitting (6) to the DCT data as shown for three typical temperatures in Fig. 21, we find that $N = 1$ for all values of T_{base}.

The Arrhenius plot is constructed following the steps below.

1. After identifying the dominant time constants from the measurement data and assuming that the lattice temperature is the same as the baseplate temperature, we construct an initial Arrhenius plot. Further, we assume that the trap properties for the DCT are the same as those based on DC Fe and C properties of the sample.
2. Then, we extract the peak lattice temperature of the device from DCT TCAD simulations.
3. The temperature of the Arrhenius plot is updated assuming that the time constants were unaltered.
4. We update two trap properties from Arrhenius extraction, specifically the energy of the deep level as well as electron capture cross section, and reuse them to re-run the DCT TCAD simulations.
5. Steps 2. to 4. are repeated until the highest temperature stabilizes.

From this workflow, we found that the Joule heating for the transient case is on the order of 10 K, so the convergence typically takes only one self-consistent iteration. The energy of the extracted trap signature is very likely of a point defect, *i.e.*, electron acceptor trap, according to Fig. 22. Note that the 298 K data point is the only temperature excluded from the Arrhenius fit because the traps emit/capture slower, so the output current signal in the measurements and TCAD did not stabilize at the end of the DCT emission phase. Moreover, the activation energy, E_a, of the extracted trap aligns with that of Fe [21], which further confirms the electron acceptor nature of the trap. The extracted E_a and capture cross-section (σ_n) are adopted in TCAD for the deep level Fe electron traps.

2) DCT Normalized Result: With Fe trap properties obtained from the Arrhenius plot, the DCT characteristics can be calibrated across all temperatures, and here fittings for three typical temperatures are presented in Fig. 23. The fits are normalized to minimum and maximum current levels measured experimentally, so our models capture only the temporal features of the data. This is because the fabricated HEMT for the DCT

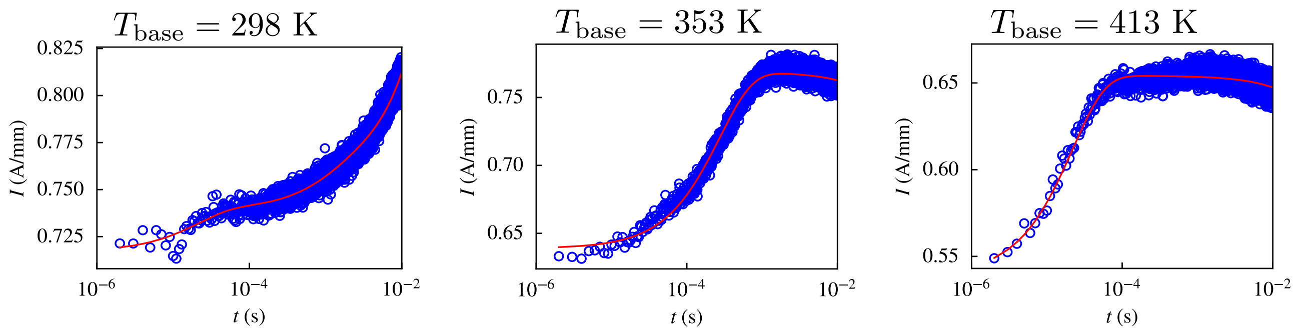

Fig. 21. (lines) Fits with single exponential + DC component to (symbols) experiment drain current transients at $T_{\rm base}$ = (left) 298 K, (middle) 353 K and (right) 413 K.

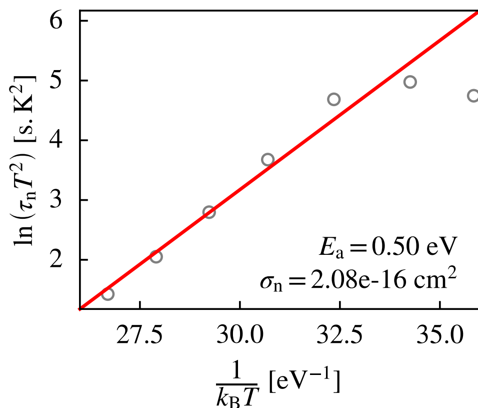

Fig. 22. Arrhenius plot constructed from the fits in Fig. 21.

measurement has slightly different gate width and different number of fingers compared to the sample used for DC measurements. This means that the specific current levels of the two samples will differ, but the impact of traps (*i.e.*, their time-domain response) is expected to be the same. With increased $T_{\rm base}$, the emission of electrons from the trap states accelerates, leading to an early onset of increase in current magnitude. The initial collapse of normalized current ($I_{\rm norm}$) observed in TCAD simulations can correspond to many physical reasons including but not limited to the faster electron capture process due to the shallow UID before emission processes take place since it is not fully occupied yet at the beginning as shown in Fig. 24, and is widely observed in literature as well [43]–[45]. Our TCAD simulations show stable current at long time scales, while measurement data shows a slight decrease in current or $T_{\rm base} = \{333, 353, 373, 393, 413\}$ K. This discrepancy indicates that the heat dissipation of experimental samples is worse than theoretically captured, and/or there are slower traps in the sample that were not fully identified from the DCT data since the measurement period was not sufficiently long.

IV. Conclusion

We performed 2-D TCAD electro-thermal simulations of a fabricated AlGaN/GaN HEMT grown on SiC substrate. The DC simulation were conducted assuming drift diffusion theory coupled with Fourier's heat and Poisson's equation accounting for compensation doping in the HEMT. Inclusion of forward gate leakage current via thermionic emission was shown to be necessary to account for negative drain current at low $V_{\rm d}$ and high $V_{\rm g}$. We investigated appropriate thermal boundary conditions of our DUT. We showed that only adjusting the bulk conductivities of the various epitaxial layers was insufficient to capture the heat flow accurately, rather the metal electrodes with an appropriate thermal conductance were required to achieve the desired heat dissipation in the DUT. DCT simulations with the same set of parameters and formulations as DC are also performed to specifically calibrate deep-level Fe trap properties. From the Arrhenius plot extracted through sum of exponentials fitted to measurements, activation energy and capture cross-section of the trap is determined. Using these properties, qualitative fits between transient TCAD and experiments are achieved, and we observe the same onset time of emission current between them as well as a lattice heating (on the order of only 10 K) much less prominent than DC, further reassuring that the DCT signature is due to existence of Fe in our DUTs and that the thermal reliability is not compromised.

References

[1] N. Islam, M. F. P. Mohamed, M. F. A. J. Khan, S. Falina, H. Kawarada, and M. Syamsul, "Reliability, applications and challenges of gan hemt technology for modern power devices: A review," *Crystals*, vol. 12, no. 11, p. 1581, 2022.

[2] O. Ambacher, B. Christian, M. Yassine, M. Baeumler, S. Leone, and R. Quay, "Polarization induced interface and electron sheet charges of pseudomorphic scaln/gan, gaaln/gan, inaln/gan, and inaln/inn heterostructures," *Journal of Applied Physics*, vol. 129, no. 20, 2021.

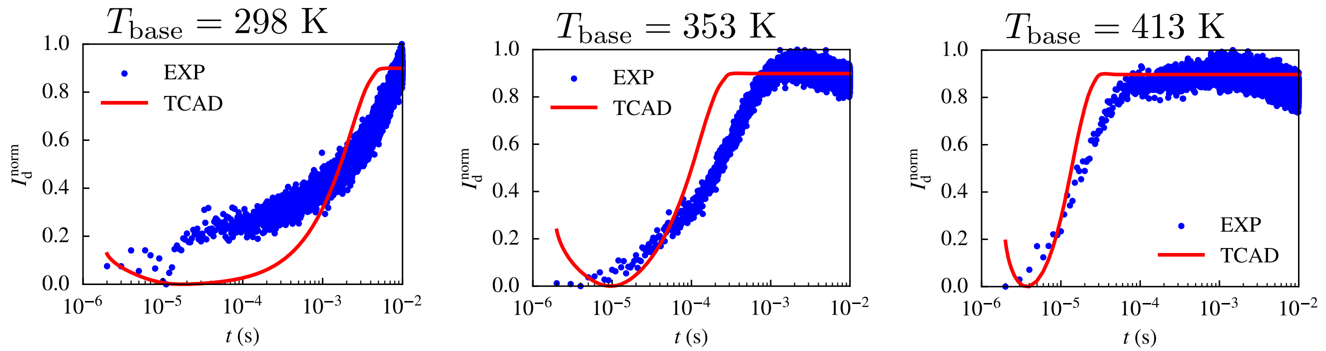

Fig. 23. Normalized TCAD and experiment drain current transients at T_{base} = (left) 298 K, (middle) 353 K and (right) 413 K. TCAD maximum value tops at 90% to account for thermal noise in the measured output current.

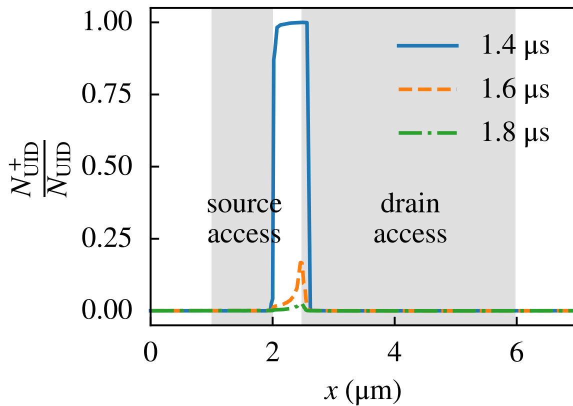

Fig. 24. UID occupancy with time along the channel which exhibits fast capture of electrons before the emission phase at time of 2 µs.

[3] M. Shur, B. Gelmont, and M. Asif Khan, "Electron mobility in two-dimensional electron gas in aigan/gan heterostructures and in bulk gan," *Journal of electronic materials*, vol. 25, pp. 777–785, 1996.

[4] L. Ardaravičius, A. Matulionis, J. Liberis, O. Kiprijanovic, M. Ramonas, L. Eastman, J. Shealy, and A. Vertiatchikh, "Electron drift velocity in algan/gan channel at high electric fields," *Applied Physics Letters*, vol. 83, no. 19, pp. 4038–4040, 2003.

[5] J. Moon, M. Micovic, P. Janke, P. Hashimoto, W.-S. Wong, R. Widman, L. McCray, A. Kurdoghlian, and C. Nguyen, "Gan/algan hemts operating at 20 ghz with continuous-wave power density¿ 6 w/mm," *Electronics Letters*, vol. 37, no. 8, pp. 528–530, 2001.

[6] b. H. Morkoc, S. Strite, G. Gao, M. Lin, B. Sverdlov, and M. Burns, "Large-band-gap sic, iii-v nitride, and ii-vi znse-based semiconductor device technologies," *Journal of Applied physics*, vol. 76, no. 3, pp. 1363–1398, 1994.

[7] T. Maeda, T. Narita, H. Ueda, M. Kanechika, T. Uesugi, T. Kachi, T. Kimoto, M. Horita, and J. Suda, "Parallel-plane breakdown fields of 2.8-3.5 mv/cm in gan-on-gan pn junction diodes with double-side-depleted shallow bevel termination," in *2018 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2018, pp. 30–1.

[8] A. Kyuregyan and S. Yurkov, "Room-temperature avalanche breakdown voltages of p-n# 3 junctions made of si, ge, sic, gaas, gap, and inp," *Soviet Physics–Semiconductors(English Translation)*, vol. 23, no. 10, pp. 1126–31, 1989.

[9] Q. Zheng, C. Li, A. Rai, J. H. Leach, D. A. Broido, and D. G. Cahill, "Thermal conductivity of gan, gan 71, and sic from 150 k to 850 k," *Physical Review Materials*, vol. 3, no. 1, p. 014601, 2019.

[10] G. Nolas and H. Goldsmid, "Thermal conductivity of semiconductors," in *Thermal Conductivity: Theory, Properties, and Applications*. Springer, 2004, pp. 105–121.

[11] E. Ziade, J. Yang, G. Brummer, D. Nothern, T. Moustakas, and A. J. Schmidt, "Thickness dependent thermal conductivity of gallium nitride," *Applied Physics Letters*, vol. 110, no. 3, 2017.

[12] J.-H. Wang, X.-H. Wang, L. Pang, X.-J. Chen, and X.-Y. Liu, "Modeling, simulation and analysis of thermal resistance in multi-finger algan/gan hemts on sic substrates," *Chinese Physics Letters*, vol. 29, no. 8, p. 088502, 2012.

[13] R. Pearson, B. Chatterjee, S. Kim, S. Graham, A. Rattner, and S. Choi, "Guidelines for reduced-order thermal modeling of multifinger gan hemts," *Journal of Electronic Packaging*, vol. 142, no. 2, p. 021012, 2020.

[14] A. Darwish, A. J. Bayba, and H. A. Hung, "Channel temperature analysis of gan hemts with nonlinear thermal conductivity," *IEEE Transactions on electron devices*, vol. 62, no. 3, pp. 840–846, 2015.

[15] J. Cho, Y. Li, D. H. Altman, W. E. Hoke, M. Asheghi, and K. E. Goodson, "Temperature dependent thermal resistances at gan-substrate interfaces in gan composite substrates," in *2012 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. IEEE, 2012, pp. 1–4.

[16] R. Menozzi, G. A. Umana-Membreno, B. D. Nener, G. Parish, G. Sozzi, L. Faraone, and U. K. Mishra, "Temperature-dependent characterization of algan/gan hemts: Thermal and source/drain resistances," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 2, pp. 255–264, 2008.

[17] J. Kuzmík, S. Bychikhin, M. Neuburger, A. Dadgar, A. Krost, E. Kohn, and D. Pogany, "Transient thermal characterization of algan/gan hemts grown on silicon," *IEEE Transactions on Electron Devices*, vol. 52, no. 8, pp. 1698–1705, 2005.

[18] T. Wittberg, "Barium adsorption on nickel: Auger electron spectroscopy and work-function measurements," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 9, no. 4, pp. 2400–2401, 1991.

[19] C. G. Van de Walle, C. Stampfl, and J. Neugebauer, "Theory of doping and defects in iii–v nitrides," *Journal of crystal growth*, vol. 189, pp. 505–510, 1998.

[20] C. Seager, A. Wright, J. Yu, and W. Götz, "Role of carbon in gan," *Journal of applied physics*, vol. 92, no. 11, pp. 6553–6560, 2002.

[21] A. Polyakov, N. Smirnov, A. Govorkov, T. Yugova, A. Markov, A. Dabiran, A. Wowchak, B. Cui, J. Xie, A. Osinsky *et al.*, "Electrical properties of gan (fe) buffers for algan/ gan high electron mobility transistor structures," *Applied physics letters*, vol. 92, no. 4, 2008.

[22] M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur, *Properties of Advanced Semiconductor Materials: GaN, AIN, InN, BN, SiC, SiGe*. John Wiley & Sons, 2001.

[23] C. Canali, G. Majni, R. Minder, and G. Ottaviani, “Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature,” *IEEE Transactions on electron devices*, vol. 22, no. 11, pp. 1045–1047, 1975.

[24] S. Bajaj, T.-H. Hung, F. Akyol, D. Nath, and S. Rajan, “Modeling of high composition algan channel high electron mobility transistors with large threshold voltage,” *Applied Physics Letters*, vol. 105, no. 26, 2014.

[25] S. Bajaj, O. F. Shoron, P. S. Park, S. Krishnamoorthy, F. Akyol, T.-H. Hung, S. Reza, E. M. Chumbes, J. Khurgin, and S. Rajan, “Density-dependent electron transport and precise modeling of gan high electron mobility transistors,” *Applied Physics Letters*, vol. 107, no. 15, 2015.

[26] J. Khurgin, Y. J. Ding, and D. Jena, “Hot phonon effect on electron velocity saturation in gan: A second look,” *Applied physics letters*, vol. 91, no. 25, 2007.

[27] S. Turuvekere, D. S. Rawal, A. DasGupta, and N. DasGupta, “Evidence of fowler–nordheim tunneling in gate leakage current of algan/gan hemts at room temperature,” *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4291–4294, 2014.

[28] I. Jabbari, M. Baira, H. Maaref, and R. Mghaieth, “Evidence of poole-frenkel and fowler-nordheim tunneling transport mechanisms in leakage current of (pd/au)/al0. 22ga0. 78n/gan heterostructures,” *Solid State Communications*, vol. 314, p. 113920, 2020.

[29] J. Liang, L. Lai, Z. Zhou, J. Zhang, J. Zhang, J. Xu, Y. Zhang, X. Liu, and W. Luo, “Trap-assisted tunneling current of ultrathin inaln/gan hemts on si (1 1 1) substrate,” *Solid-State Electronics*, vol. 160, p. 107622, 2019.

[30] K. Li, E. Yagyu, H. Saito, K. H. Teo, and S. Rakheja, “Compact modeling of gate leakage phenomenon in gan hemts,” in *2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*. IEEE, 2020, pp. 225–228.

[31] T. E. Beechem, A. E. McDonald, E. J. Fuller, A. A. Talin, C. M. Rost, J.-P. Maria, J. T. Gaskins, P. E. Hopkins, and A. A. Allerman, “Size dictated thermal conductivity of gan,” *Journal of Applied Physics*, vol. 120, no. 9, 2016.

[32] C. Uher, *Thermal Conductivity of Metals*. Boston, MA: Springer US, 2004, pp. 21–91. [Online]. Available: https://doi.org/10.1007/0-387-26017-X_2

[33] H. Gomi, T. Yoshino *et al.*, “Resistivity, seebeck coefficient, and thermal conductivity of platinum at high pressure and temperature,” *Physical Review B*, vol. 100, no. 21, p. 214302, 2019.

[34] A. Hasegawa, K. Ohta, T. Yagi, and K. Hirose, “Thermal conductivity of platinum and periclase under extreme conditions of pressure and temperature,” *High Pressure Research*, vol. 43, no. 1, pp. 68–80, 2023.

[35] J. Cook and M. v. d. Meer, “The thermal conductivity and electrical resistivity of gold from 80 to 340 k,” *Canadian Journal of Physics*, vol. 48, no. 3, pp. 254–263, 1970.

[36] R. Powell and R. Tye, “The thermal and electrical conductivity of titanium and its alloys,” *Journal of the less Common Metals*, vol. 3, no. 3, pp. 226–233, 1961.

[37] D. K. Schroder, “Contact resistance and Schottky barriers,” in *Semiconductor Material and Device Characterization*. IEEE Press Wiley-Interscience, 2006, pp. 127–184.

[38] J. Kuzmik, J.-F. Carlin, M. Gonschorek, A. Kostopoulos, G. Konstantinidis, G. Pozzovivo, S. Golka, A. Georgakilas, N. Grandjean, G. Strasser *et al.*, “Gate-lag and drain-lag effects in (gan)/inaln/gan and inaln/aln/gan hemts,” *physica status solidi (a)*, vol. 204, no. 6, pp. 2019–2022, 2007.

[39] P. Löw, B. Kim, N. Takama, and C. Bergaud, “High-spatial-resolution surface-temperature mapping using fluorescent thermometry,” *Small*, vol. 4, no. 7, pp. 908–914, 2008.

[40] L. Shi and A. Majumdar, “Recent developments in micro and nanoscale thermometry,” *Microscale Thermophysical Engineering*, vol. 5, no. 4, pp. 251–265, 2001.

[41] S. Ippolito, S. Thorne, M. Eraslan, B. Goldberg, M. Ünlü, and Y. Leblebici, “High spatial resolution subsurface thermal emission microscopy,” *Applied Physics Letters*, vol. 84, no. 22, pp. 4529–4531, 2004.

[42] D. Bisi, M. Meneghini, C. De Santi, A. Chini, M. Dammann, P. Brueckner, M. Mikulla, G. Meneghesso, and E. Zanoni, “Deep-level characterization in gan hemts-part i: Advantages and limitations of drain current transient measurements,” *IEEE Transactions on electron devices*, vol. 60, no. 10, pp. 3166–3175, 2013.

[43] J. M. Tirado, J. L. Sanchez-Rojas, and J. I. Izpura, “Trapping effects in the transient response of algan/gan hemt devices,” *IEEE Transactions on Electron Devices*, vol. 54, no. 3, pp. 410–417, 2007.

[44] G. Meneghesso, M. Meneghini, D. Bisi, I. Rossetto, A. Cester, U. K. Mishra, and E. Zanoni, “Trapping phenomena in algan/gan hemts: A study based on pulsed and transient measurements,” *Semiconductor science and technology*, vol. 28, no. 7, p. 074021, 2013.

[45] K. Sehra, V. Kumari, M. Gupta, M. Mishra, D. Rawal, and M. Saxena, “Tcad investigation of gate-lag measurements on conventional and π-gate algan/gan hemts,” in *2020 IEEE 20th International Conference on Nanotechnology (IEEE-NANO)*. IEEE, 2020, pp. 128–133.