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Abstract

GaN HEMTs plays a vital role in high-power and high-frequency electronics. Meeting the demanding performance requirements of these devices without compromising reliability is a challenging endeavor. Field Plates are employed to redistribute the electric field, minimizing the risk of device failure, especially in high-voltage operations. While machine learning has been applied to GaN device design, its application to field plate structures, known for their geometric complexity, is limited. This study introduces a novel approach to streamlining the field plate design process. It transforms complex 2D field plate 2 structures into a concise feature space, reducing data requirements. A machine learning- assisted design framework is proposed to optimize field plate structures and perform inverse design. This approach is not exclusive to the design of GaN HEMTs and can be extended to various semiconductor devices with field plate structures. The framework combines technology computer-aided design (TCAD), machine learning, and optimization, streamlining the design process.

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Keywords: GaN, Field Plate, Machine Learning, TCAD, Inverse Design

Abstract— GaN HEMTs plays a vital role in high-power and high-frequency electronics. Meeting the demanding performance requirements of these devices without compromising reliability is a challenging endeavor. Field Plates are employed to redistribute the electric field, minimizing the risk of device failure, especially in high-voltage operations. While machine learning has been applied to GaN device design, its application to field plate structures, known for their geometric complexity, is limited. This study introduces a novel approach to streamlining the field plate design process. It transforms complex 2D field plate

structures into a concise feature space, reducing data requirements. A machine learning-assisted design framework is proposed to optimize field plate structures and perform inverse design. This approach is not exclusive to the design of GaN HEMTs and can be extended to various semiconductor devices with field plate structures. The framework combines technology computer-aided design (TCAD), machine learning, and optimization, streamlining the design process.

1. Introduction

GaN High Electron Mobility Transistors (HEMTs) have found extensive use in high-power and high-frequency electronic devices, including chargers,[1] RF,[2,3] and microwave power applications [4]. Meeting the performance demands of these applications without compromising reliability requires innovative design approaches. Particularly in high-voltage operation, the risk of device failure is concentrated near the gate edge due to the higher electric field. To mitigate this risk, Field Plates are employed to distribute the electric field along the channel, reducing the peak electric field and enhancing device reliability [6-10]. Recent efforts have combined Technology Computer-Aided Design (TCAD) with machine learning and optimization techniques to optimize GaN device design [11-14]. However, most of these endeavors have focused on relatively simple device structures, characterized by a limited set of design parameters. Field plates, on the other hand, exhibit substantial geometric variations that present challenges for applying artificial intelligence (AI) methods in their design. Previous study have demonstrated the optimization of field plates to achieve high breakdown voltage using Artificial Neural Networks [24]. However, these methods have proved less flexible in terms of the field plate structure and have not achieved the desired optimization for other crucial parameters such as gate-drain capacitance and leakage current.

In this study, we present a novel approach for transforming complex field plate structures into a concise feature space, enabling their integration into machine learning models with minimal data requirements. We subsequently propose a machine learning-assisted design framework aimed at optimizing field plate structures to achieve a desired blocking voltage while ensuring reasonable gate-drain capacitance and leakage current. This approach, which includes inverse design, offers a promising solution to address this unique design challenge. This approach is not only effective for GaN HEMTs but also easily transferable to other

transistors featuring field plate structures, such as Si [15-16], SiC [17-19] and GaAs [20-22]. Through appropriate feature engineering, this methodology extends its applicability across a broad range of semiconductor devices. Compared to traditional response surface methodology (RSM) or other design of experiments (DOE) method, this TCAD+AI strategy largely reduces the technology development time and provide more functionalities.

2. TCAD Simulation

Sentaurus TCAD is used to simulate GaN HEMT device. The TCAD model, provided by Synopsys, has been meticulously calibrated to match experimental data [5]. Specifically, the relationship between carrier saturation velocity (v_{sat}) and sheet charge densities (n_{sh}) has been accurately calibrated against experimental results via high-field saturation model (Caughey-Thomas model). Additionally, trap densities are used to calibrate the carbon profiles in the carbon-doped buffer and channel regions to match experimental data closely (3.30e18 cm^{-3} acceptor defect, energy level 0.9 eV from valence band and 1.70e18 cm^{-3} donor defect, energy level 0.4 eV from conduction band in buffer region; 5.28e16 cm^{-3} acceptor defect, energy level 0.9 eV from valence band and 2.72e16 cm^{-3} donor defect, energy level 0.3 eV from conduction band in channel region; 3.8e12 cm^{-3} donor defect, energy level from 1.29 eV to 1.45 eV from midgap using uniform distribution, 4.7e12 cm^{-3} donor defect, energy level from 1.15 eV to 1.29 eV from midgap using uniform distribution, 2.4e12 cm^{-3} donor defect, energy level from 0.99 eV to 1.15 eV from midgap using uniform distribution, 1.4e12 cm^{-3} donor defect, energy level from 0.75 eV to 1.99 eV from midgap using uniform distribution at interface of GaN/Nitride). Other parameters, such as subthreshold swing (≈210 mV/decade), drain-induced barrier lowering (DIBL) effects (≈45 mV/V) and the sheet charge densities in these regions are also carefully calibrated (≈7.4e12 cm^{-2}). Furthermore, the relationship between carrier mobility under low electric field conditions and sheet charge densities simulated by the inversion and accumulation layer mobility model (IALMob) has been aligned with experimental observations. Doping-dependent mobility model is also turned on to further improve mobility values. The I_D-V_{GS} and I_D-V_{DS} curves show good agreement with experimental data (Fig. 1), ensuring the reliability of our simulation model for the GaN HEMT devices studied.

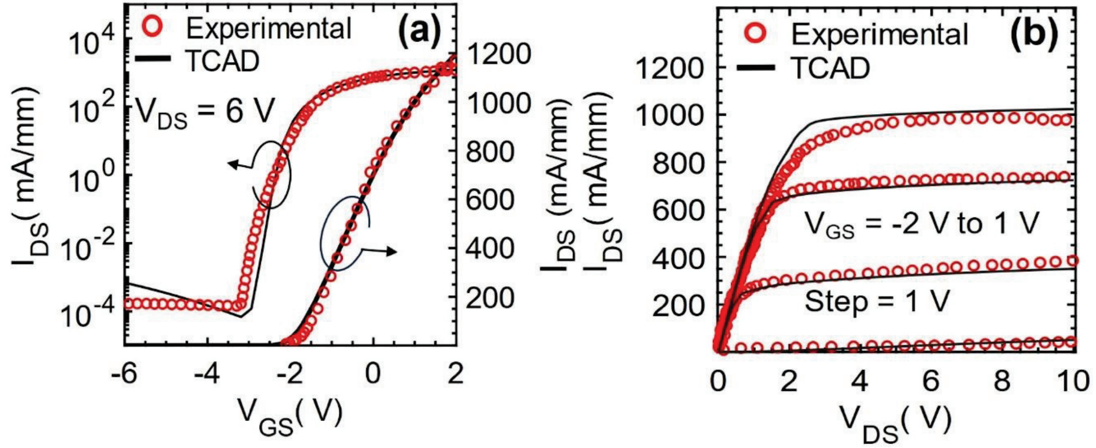


Figure 1. Calibration of TCAD simulation models based on experimental data from [5] (a) I_D-V_{GS} (b) I_D-V_{DS} characteristics. All relevant physics models such as Doping Dependent Mobility, Caughey-Thomas Model, Fermi statistic for carrier density calculation, Thermionic emission for charge injection, SRH Recombination (both hole and electron capture cross sections are set to be 1e-15 cm^2) and Piezoelectric Polarization (strain activation is 1.0 at barrier/channel, 0.1 at cap layer/barrier and 0.05 at GaN/Nitride) are included [23]. An excellent match is observed.

Using the calibrated model parameters for GaN HEMT mentioned before, a typical device structure was developed using Synopsys Sentaurus TCAD tool. The structure is shown in Fig. 2. From bottom to top, the device consists of a SiC substrate, 0.1 μm AlN seed layer, 2.0 μm GaN buffer layer, 0.05 μm GaN channel layer built from epitaxy growth model, 0.02 μm AlGaN barrier layer built from epitaxy growth mode, 0.002 μm GaN cap layer, 0.1 μm Si_3N_4 nitride layer and 0.2 μm oxide layer. Among these layers, channel layer, barrier layer, and cap layer are built from epitaxy growth model. To focus on field plate design, we fix the separation between source and gate to be 1.0 μm and separation between gate and drain to be 2.0 μm. Lengths of source, gate and drain are fixed to be 0.5 μm, 0.35 μm and 0.5 μm, respectively. Intentional rounding of contact corners during gate formation is employed to facilitate controlled tunneling and achieve a closer resemblance to practical applications.

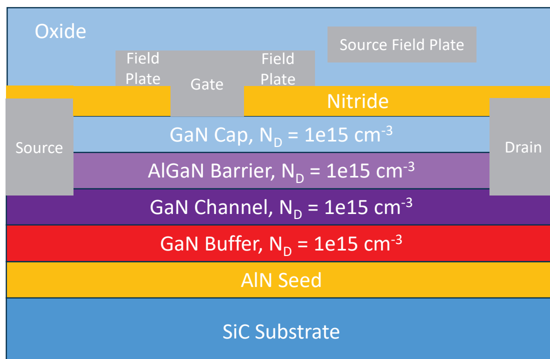


Figure 2. Schematic of GaN HEMT device structure in TCAD Simulation

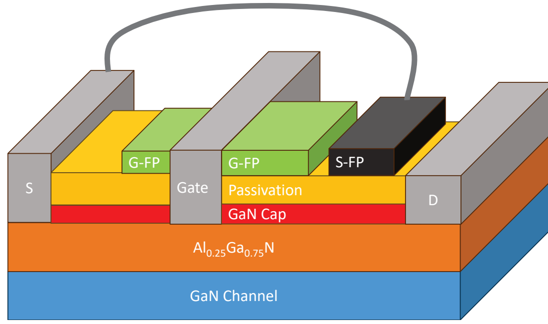


Figure 3. A 3D representation of a GaN HEMT device featuring a field plate designed using the method described in this work.

In Fig. 2, Two types of field plate structures are being considered: gate-connected field plate and source-connected field plate. The left side length of gate connected field plate L_{gp} is fixed to be 0.4 μm as it has a minimal impact on blocking voltage optimization. Conversely, the right-side length of the gate field plate and the thickness of the gate metal are adjustable. Regarding the source field plate structure, the horizontal location, vertical location, and field plate thickness can vary. A 3D representation of our designed GaN HEMT device is shown in Fig. 3.

Three key device performance metrics are extracted from TCAD simulations: off-state blocking voltage (BV), gate-drain capacitance (C_{gd}), and gate leakage. We use a standard scheme from [23] to obtain BV. As for C_{gd}, an AC simulation is conducted at the threshold voltage under zero drain bias with a frequency of 5 GHz. The gate leakage measurement is performed with the device in an off-state and a drain voltage of 24 V. A total of 488 TCAD simulations were generated under these specific settings.

3. Feature Engineering

One of the key success factors for machine learning models is feature engineering. The challenge in this work is how to convert field plate structure into features which can be efficiently captured and learned in a ML model. To streamline the analysis, we initially project the 2D field plate structure and metal contact into one-dimensional arrays, as depicted in Fig. 4(a). Each unit within these arrays represents various aspects of the field plate, such as metal plate thickness and oxide thickness above or below it. This transformation results in a 3 x N matrix, where N corresponds to the number of units in each array, based on the chosen resolution. The resolution N was selected based on a balance between computational feasibility and the ability to capture relevant geometrical features of the field plate structures.

For instance, with a transistor width of 4 μm and a resolution of 0.05 μm, which is sufficient to capture the geometrical features of field plates, each array comprises 80 features. This necessitates a substantial quantity of TCAD runs or experimental data to develop a reliable input to the machine learning model. The geometric aspects of field plates optimized in our study include metal plate thickness of gate and source-connected field plate (parameterized by T_{gp} and T_{sfp}), oxide thickness below the source connected field plate (parameterized by T_{oxide}), length, horizontal and vertical positions of both gate and source connected field plates (parameterized by combination of R_{gp}, Loc_{sfp_left} and Loc_{sfp_right}).

(a)

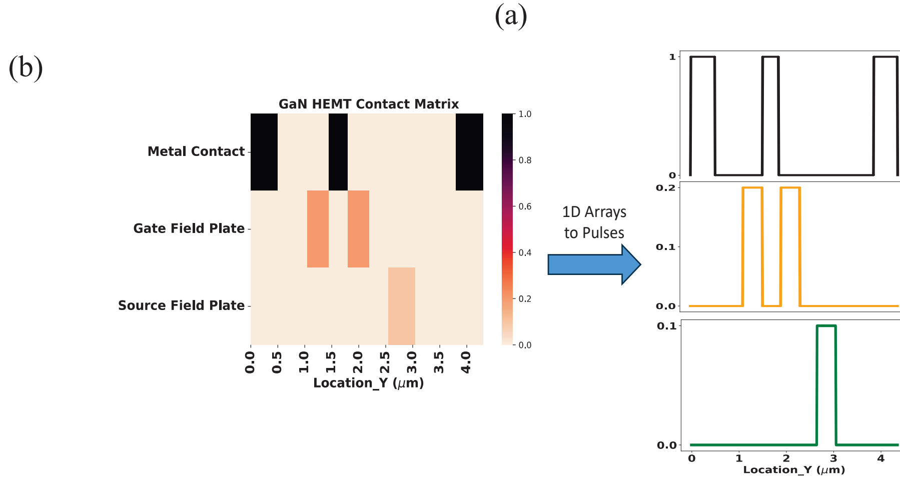


Figure 4. 2D Field Plate Geometry Transformation Process

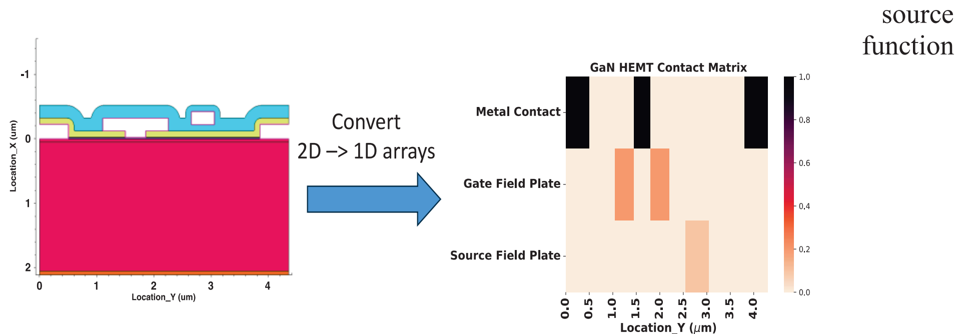
To address this data challenge, we implement a second transformation, as depicted in Fig. 4(b). We convert the 1D arrays into a series of pulse functions, which is particularly effective given the sparse nature of the 1D feature array. In the example provided earlier, the metal plate array is transformed into three rectangular pulse functions, each requiring only two parameters (the left and right electrode locations):

$$F_{metal\ plate}(x) = Rect(x;\ Electrode\ Left, Electrode\ right)$$

The gate field plate array is transformed into two rectangular pulse functions, with just three parameters (Metal Thickness, Gate Field Plate Left and Gate Field Plate Right) for each function needed to represent the metal thickness and the field plate's location:

$$F_{gate\ plate}(x) = Metal\ Thickness * Rect(x;\ Gate\ Field\ Plate\ Left, Gate\ Field\ Plate\ Right)$$

Similarly, the source plate pulse function requires three parameters:



$$F_{source\ plate}(x) = Oxide\ Thickness * Rect(x;\ Source\ Field\ Plate\ Left, Source\ Field\ Plate\ Right)$$

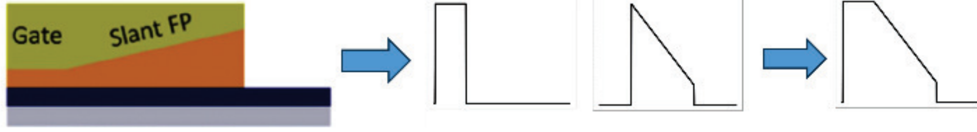


Figure 5. Convert slant field plate into a pulse function via coupling of rectangular and sawtooth pulse functions.

For more intricate field plate structures, such as a slant field plate shown in Fig. 5, we can employ triangular, sawtooth, Gaussian, or other pulse functions to decode the field plate's configuration. This method significantly reduces feature dimensions while retaining sufficient information for effective machine learning. It is important to note that as the complexity of the field plate structures increases, resulting in higher feature dimensions, more data is required to train the neural network surrogate model effectively. In our study, we considered 6 features, in which T_{gp} ranges from 0.2 µm to 0.6 µm, T_{sfp} ranges from 0 to 0.6 µm, T_{oxide} ranges from 0 to 0.2 µm, R_{gp} ranges from 0.2 µm to 1.6 µm, Loc_{sfp_left} ranges from 2.35 µm to 3.25 µm, L_{sfp} ranges from 0 µm to 1.2 µm ($Loc_{sfp_right} = Loc_{sfp_left} + L_{sfp}$), and L_{gp} is kept at 0.4 µm. Slant field plate is not included. Around 500 TCAD simulations were sufficient to train a well-performing model, which took about a month of CPU time. When the number of features doubles, we anticipate that the required TCAD data will also double to achieve a robust model. However, running TCAD simulations on a computer cluster with multiple CPUs can significantly reduce the training time. While the training time of the neural network surrogate model increases with more data and features, this process takes less than 10 minutes on one GPU for our current model, and the execution time of the neural network model is faster, typically completed in 5 minutes. Therefore, we expect the most time-consuming step to be the TCAD data generation. Thus, while the generation of TCAD data is the most time-consuming step, the overall process remains manageable. Based on our observations, we estimate that optimizing up to 70-80 metrics with acceptable complexity is feasible in one month if leveraging parallel computing resources (> 8 CPUs) for TCAD data generation.

4. AI-assisted Design Framework

Following the feature transformation, we utilized the TCAD dataset to train a robust neural network surrogate model, the hyperparameter of which is optimized via Bayesian

Optimization. The dataset was divided into 80% for training and 20% for validation and testing. Fig. 6 provides an overview of the neural network model's architecture, featuring three output layers, each responsible for predicting one of the performance metrics. The training and validation results are presented in Fig. 7 and Table 1. These results demonstrate the model's capability to well predict key metrics, including BV, C_{gd}, and gate leakage except for that the BV prediction in the high BV region is saturated due to the lack of BV data in high BV region. This is also reported in other literature [12].

Subsequently, we employ an AI-assisted framework, illustrated in Fig. 8 and Fig. 9, The neural network model is then integrated into the NSGA-II optimization framework as an optimization problem to co-optimize three key performance metrics of GaN HEMT devices: blocking voltage, gate leakage, and capacitance. These three metrics are optimized under the constraints of physical dimension of device structures. Optimizing gate leakage reduces power dissipation, leading to more efficient operation. Reducing C_{gd} capacitance increases the speed of operation and further improves efficiency. Additionally, a high BV allows MOSFETs to operate safely in high-voltage environments, which is critical for applications such as power supplies, motor drives, and inverters where high voltages are common. This comprehensive optimization ensures that the MOSFETs deliver enhanced performance across various metrics while maintaining reliability and efficiency. There are two optimization strategies. The first in Fig. 8 aims to optimize all three metrics, which involves maximizing BV while minimizing gate leakage and C_{gd}. The second strategy in Fig. 9 targets a specific BV value while minimizing gate leakage and C_{gd}. The latter approach is commonly known as inverse design. The algorithm is illustrated in following equations:

$max\ f_{BV}(x;\ F_{metal\ plate}, F_{gate\ plate}, F_{source\ plate})$ or

$min\ abs(Target\ BV - f_{BV}(x;\ F_{metal\ plate}, F_{gate\ plate}, F_{source\ plate}))$ for inverse design

$min\ f_{gate_leakage}(x;\ F_{metal\ plate}, F_{gate\ plate}, F_{source\ plate})$

$min\ f_{C_{gd}}(x;\ F_{metal\ plate}, F_{gate\ plate}, F_{source\ plate})$

Subject to:

$Source\ Field\ Plate\ Right < Left\ of\ Drain$

$Source\ Field\ Plate\ Left > Gate\ Field\ Plate\ Left$

$Source\ Field\ Plate\ Right - Source\ Field\ Plate\ Left > 0$

To further enhance the performance of surrogate model, we will let the surrogate model acquire new information from Usage I and II and do an Incremental Learning (shown in Fig. 10).

The framework can produce Pareto front points, as demonstrated as blue dots in Fig. 11 and Fig. 12, representing potential optimal solutions. Subsequently, these solutions are subjected to validation via TCAD models. The validation results from TCAD provide

feedback to the system, which allows us to tune the neural network model to the best performance.

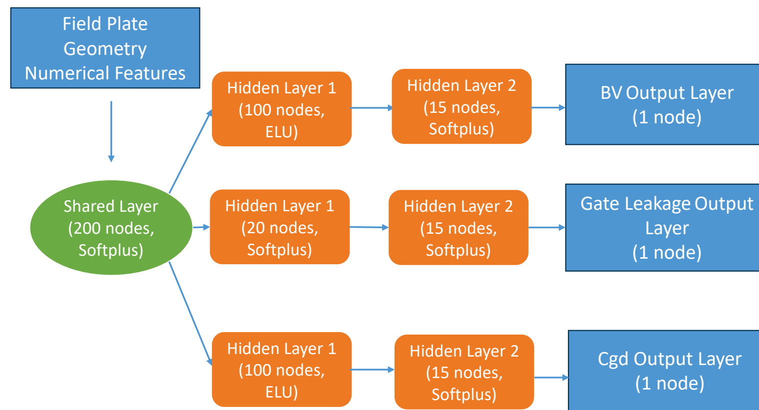


Figure 6. Architecture of Neural Network Model.

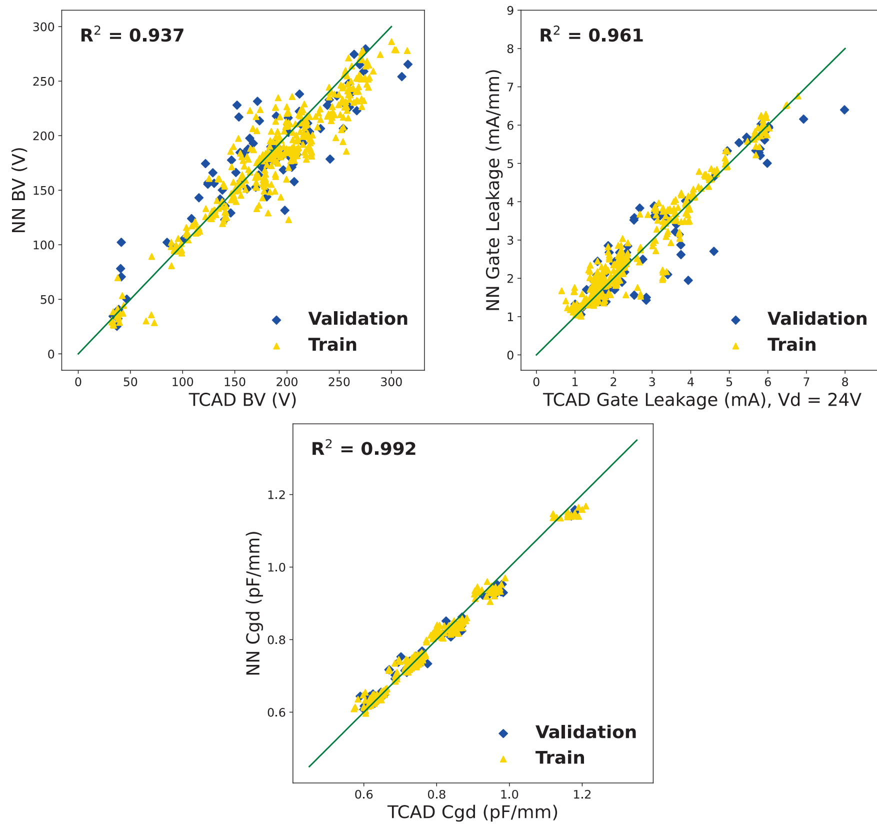


Figure. 7 Training (yellow) and validation (blue) parity plots of the NN model. Green lines show ideal predictions where NN Predication is equal to TCAD. The R^2 of the whole dataset is shown on the top left.

	Blocking Voltage (V)	Gate Leakage (mA/mm)	C_{gd} (pF/mm)
Training RMSE	20.83	0.36	1.76e-2
Validation RMSE	27.75	0.59	2.10e-2

Table 1. Training and validation RMSE of the NN Model

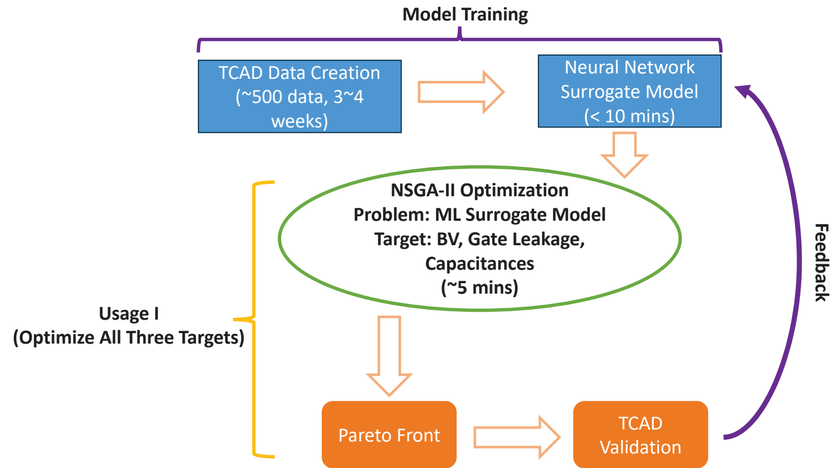


Figure 8. AI-assisted Framework of GaN HEMT Device (Training and Usage I).

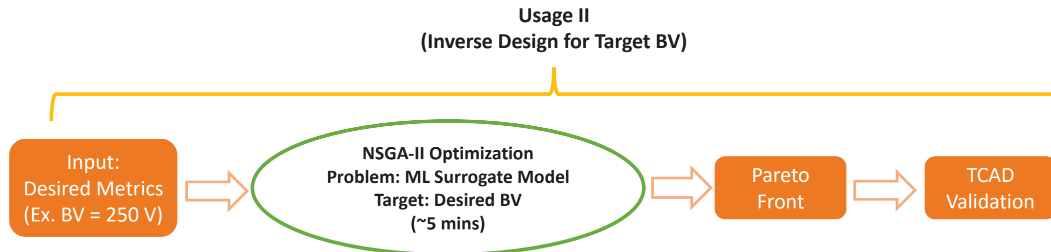


Figure 9. AI-assisted Framework of GaN HEMT Device (Usage II).

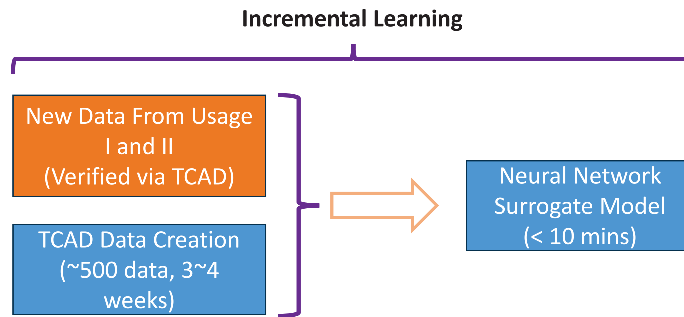


Figure 10. Incremental Learning of NN Surrogate Model.

The validation results for both optimization strategies are provided in Tables 2 and 3. These results indicate that we have been able to slightly surpass the maximum BV value in the TCAD dataset (315 V) by 1%, while effectively suppressing gate leakage by up to 23% and reducing capacitance by up to 9%. A schematic and detailed dimensions of device structure for Pareto Front 2 is shown in Fig. 13 and Table 4. It's noteworthy that the predicted BV values in the table are slightly below the maximum BV value from the TCAD data due to insufficient training data at high BV region. This implies that while the surrogate model provides a good approximation, it may not fully capture the extreme values observed in TCAD simulations due to the saturation effect. Nonetheless, it's important to highlight that our approach demonstrates the capability to exceed the maximum BV value present in the

TCAD data, suggesting that saturation mentioned in previous discussion in this section and in [12], isn't a significant concern for our optimization process. The surrogate model's predictions are still valuable for guiding the design improvements. In the context of inverse design, we set the target BV value at 250 V and obtained several feasible solutions through this framework. This not only allows us to achieve the target BV value but also optimize gate leakage and capacitance concurrently. Importantly, once a reliable AI framework is established, it significantly reduces model iteration cycles and accelerates technology development compared to traditional methods.

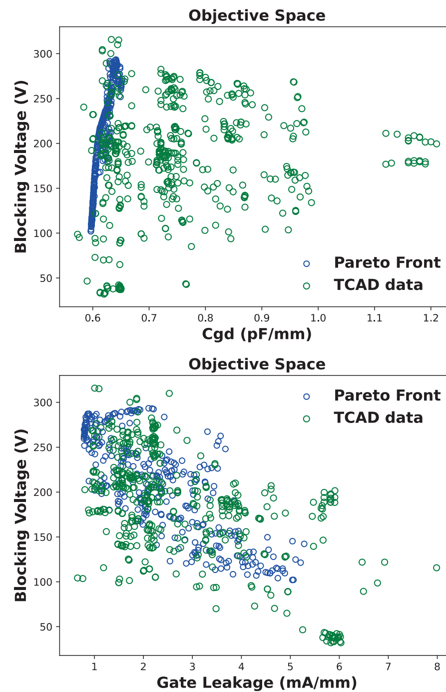


Figure 11. Pareto Front generated via AI-assisted model for device optimization. First plot shows BV vs. C_{gd} and second plot shows BV vs. gate leakage. Blue dots indicate Pareto Front, while green dots indicate TCAD simulation data.

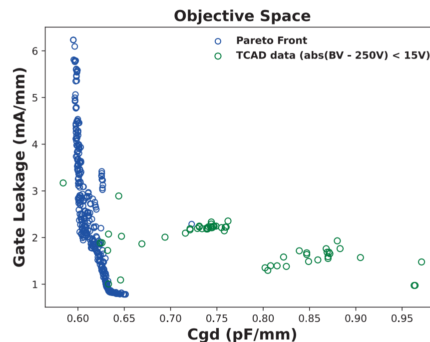


Figure 12. Pareto Front for Inverse Design of GaN HEMT with a target blocking voltage 250V (Gate leakage vs. C_{gd}). Blue dots indicate Pareto Front, while green dots indicate TCAD simulation data with BV values close to 250V.

Pareto Front	BV (NN)	Gate Leakage (NN)	C_{gd} (NN)	BV (TCAD)	Gate Leakage (TCAD)	C_{gd} (TCAD)
1	272.65	1.57	0.632	316.15	1.93	0.609
2	280.22	1.65	0.635	317.75	2.35	0.633
3	273.47	2.24	0.635	307.19	2.56	0.640
4	285.09	1.49	0.638	303.67	1.84	0.620
5	285.38	1.49	0.638	304.63	1.52	0.620
6	284.76	1.49	0.639	308.23	1.68	0.573

Table 2. NN predictions and TCAD validation results of a subset of Pareto Front for BV (V), gate leakage (mA/mm) and C_{gd} (pF/mm) optimization.

Pareto Front	Gate Leakage (NN)	C_{gd} (NN)	BV (TCAD)	Gate Leakage (TCAD)	C_{gd} (TCAD)
1	1.77	0.764	267.11	1.94	0.765
2	1.91	0.626	264.31	2.96	0.585
3	1.98	0.625	247.19	3.20	0.610
4	2.22	0.626	254.87	3.27	0.620
5	1.86	0.626	247.83	4.66	0.642

Table 3. NN prediction and TCAD validations results of a subset of Pareto Front for inverse design with target BV of 250 V. (We don't include BV results from NN model since the difference between NN BV and target BV is very small.)

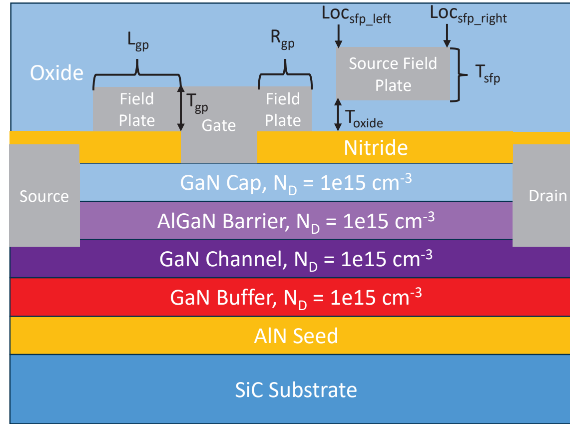


Figure 13. 2D Schematic of GaN HEMT device structure of Pareto Front 2 in Table 2, where L_{gp} denotes left side gate field plate length, R_{gp} denotes right side gate field plate length, T_{gp} denotes gate field plate thickness, Loc_{sfp_left} denotes horizontal location of left side of source field plate, Loc_{sfp_right} denotes horizontal location of right side of source field plate, T_{sfp} denotes thickness if source field plate and T_{oxide} denotes oxide layer thickness beneath source field plate.

Pareto Front	Value (μm)
L_{gp}	0.40
R_{gp}	0.20
T_{gp}	0.59
Loc_{sfp_left}	2.34
Loc_{sfp_right}	2.74
T_{sfp}	0.59
T_{oxide}	0.13

Table 4. Dimensions of device structure in Fig. 13.

5. Conclusion

In summary, this work presents a groundbreaking method to optimize semiconductor devices, focusing on GaN HEMTs and their counterparts. By transforming complex field plate structures into a concise feature space and integrating them with machine learning, we have addressed a significant challenge in semiconductor device design. The proposed AI-assisted framework effectively enhances the design and performance of GaN HEMTs, even enabling inverse design capabilities. Both two usages successfully achieve their respective goals, with the first method providing a balanced optimization of all three metrics, and the second method effectively achieving a target BV value while optimizing the other two metrics. Moreover, the approach is versatile and can be applied to other transistors featuring field plate structures, making it a valuable tool for a broad range of semiconductor devices. This work represents a promising step forward in semiconductor device design, offering efficiency and reliability to meet the demands of high-power and high-frequency electronic applications.

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