

Summary Report of International Electron Device Meeting (IEDM) 2022

Teo, Koon Hoo

TR2023-013 March 17, 2023

Abstract

Teo attended the 68th annual international Electron Device Meeting (IEDM) 2022 held in San Francisco, California, USA. The meeting is considered as the gold standard conference for reporting the latest development and breakthrough in semiconductor and device technology. This is his summary report.

Mitsubishi Electric Research Laboratories 2023

© 2023 MERL. This work may not be copied or reproduced in whole or in part for any commercial purpose. Permission to copy in whole or in part without payment of fee is granted for nonprofit educational and research purposes provided that all such whole or partial copies include the following: a notice that such copying is by permission of Mitsubishi Electric Research Laboratories, Inc.; an acknowledgment of the authors and individual contributions to the work; and all applicable portions of the copyright notice. Copying, reproduction, or republishing for any other purpose shall require a license with payment of fee to Mitsubishi Electric Research Laboratories, Inc. All rights reserved.



Summary Report of International Electron Device Meeting (IEDM) 2022

Koon Hoo Teo

March 8, 2023

Version 1.0

Executive Summary

Teo attended the 68th annual international Electron Device Meeting (IEDM) 2022 held in San Francisco, California, USA. The meeting is considered as the gold standard conference for reporting the latest development and breakthrough in semiconductor and device technology. This meeting was very well attended by the in-person conference of more than 2000 participants.

Similar to the previous years, this year conference includes areas in device design, multi-physics and device modeling, manufacturing, etc. In particular, it also includes nanometer CMOS technology, advanced novel quantum and nano-scale devices technology, optoelectronics, negative capacitance, advanced process technology and analog memory devices for AI. As for GaN technology, there were about 15 papers presented, which has one of the highest number of papers for a given technology at this meeting.

Specifically, papers using compact models of MRAM, memory devices such as ferroelectric devices, and ultra low temperature CMOS for quantum computing were presented. Models achieved uSec fast simulation using analytical functions as solutions. There were a few papers on SiC and one of which review conventional superjunction SiC power device, with the focus of using high-energy (MeV) implantations. There is also a paper on the use negative capacitance FETs which for the first time, reported the device design using a single-layer (SL)-graphene to achieve a subthreshold slope (SS) of 31 mV/dec with unnoticeable hysteresis.

As expected, Intel reported a new generation of integration architectures. Intel demonstrated that its performance includes 9x+ interconnect power reduction and density improvements.

GaN applications as usual, are chiefly divided into RF and power electronics. For power electronics, GaN device was reported to have a 10 A/cm² current density at supply voltage of 50 V, which is higher than the state-of-the-art Si devices. In another paper a 1200V/70mΩ GaN-on-sapphire devices demonstrates a high efficiency of >99% in hard-switched conditions of 900:450V buck converter at frequency of 50kHz. A vertical GaN superjunction p-n diodes are *shown for both GaN and sapphire substrates with a breakdown voltage* performance over 1100 V. A final paper on current and future potentials of vertical GaN power devices grown on GaN substrates was presented. Development of GaN bulk substrate, fundamental material properties, device epitaxial growth, advanced ion implantation and latest MOS interface are presented.

There were more paper presented on GaN for the RF applications. N polar GaN with breakthrough performance at 94GHz at 5.8W/mm with 38.5% power efficiency. Monte Carlo thermal modelling of GaN and InP devices validated by partial experimental data was reported. Both transient and steady state studies were carried out and it reveals peak temperature increases are threefold larger than conventional study using bulk diffusion. A first demonstration of GaN HEMTs for both Power and RF applications on a common platform with Fe/C Co-doped Buffer was presented. In another paper, trapping in back barrier (BB) of GaN HEMTs was examined. BB trapping is alleviated by increasing 2DEG density Nsheet concentration. A novel device BB design criterion was proposed. There is also another report on a comprehensive analysis of ESD for GaN on Si HEMTs. Transient I-V curves were verified with TCAD and pinpointed 3 different types of failure mechanisms. A heat spreader for GaN HEMTs is implemented with polycrystalline diamond. With a 500nm-thick all-around diamond, it lowers gate temperature at 9.5W/mm DC power without impact in device performances. In another paper, a high-K GaN NMOS transistor was demonstrated. A 100nm-source-field-plated with a 30nm LG GaN demonstrates a record $f_{MAX}=680GH$. In another paper, a novel Hybrid gate p-GaN power HEMT technology is proposed to enhance Vth stability. It is experimentally demonstrated that the-HEMT can achieve higher gate reliability than commercial products.

IEDM is a conference that covers many areas of semiconductor devices and technology. Though there were more than average number of papers presented on GaN at this meeting, the areas of application still only confined to RF and power electronics applications. Potentially, GaN has many more other applications, such as ultra-high and ultra-low temperature operations, audio engineering and cable applications, etc, which this meeting fails to address.

References

1. Demonstration of Analog Compute-In-Memory Using the Charge-Trap Transistor in 22 FDX Technology
S. Qiao, S. Moran, D. Srinivas, S. Pamarti, and S. S. Iyer Center for Heterogeneous Integration and Performance Scaling, Samuli School of Engineering, Electrical and Computer Engineering Department, University of California, Los Angeles (UCLA), CA 90095, USA
2. Resonant Tunneling Diode Technology for Future Terahertz Applications, S. Suzuki¹ ¹Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo Japan, email: safumi@ee.e.titech.ac.jp
3. 3D Stackable Cryogenic InGaAs HEMT-Based DC and RF Multiplexer/Demultiplexer for Large-Scale Quantum Computing , Jaeyong Jeong¹ , Seong Kwang Kim¹ , Jongmin Kim² , Jisung Lee³ , Joon Pyo Kim¹ , Bong Ho Kim¹ , Yoon-Je Suh¹ , Dae-Myeong Geum¹ , Seung-Young Park³ , and SangHyeon Kim^{1*} ¹ School of Electrical Engineering, KAIST, Daejeon, Korea *E-mail: shkim.ee@kaist.ac.kr ² Korea Advanced Nano Fab Center (KANC), Suwon, Korea, ³ Korea Basic Science Institute (KBSI), Daejeon, Korea
4. Ferroelectric and Interlayer Co-optimization with In-depth Analysis for High Endurance FeFET , Yuejia Zhou¹ , Zhongxin Liang¹ , Wenpu Luo¹ , Ming Yu¹ , Runteng Zhu¹ , Xiao Lv¹ , Jiachen Li¹ , Qianqian Huang^{1,2} , Fei Liu^{1,2} , Kechao Tang^{1,2*} , and Ru Huang^{1,2*} ¹School of Integrated Circuits, Peking University, Beijing 100871, China. email: tkch@pku.edu.cn; ruhuang@pku.edu.cn ²Beijing Advanced Innovation Center for Integrated Circuits, Beijing 100871, China.
5. Compact Modeling of Emerging IC Devices for Technology-Design Co-development , Invited Paper G. Pahwa¹ , A. Dasgupta² , C. T. Tung¹ , M.Y. Kao¹ , C. K. Dabhi¹ , S. Sarker² , S. Salahuddin¹ , C. Hu¹ ¹University of California, Berkeley, CA. USA, ² IIT-Roorkee, Roorkee, India
6. Scalable Ultrahigh Voltage SiC Superjunction Device Technologies for Power Electronics Applications , R. Ghandi¹ , C. Hitchcock¹ , S. Kennerly¹ , M. Torky² and T.P. Chow² ¹GE Research, Niskayuna, NY 12309, USA, email: gandi@ge.com ²Rensselaer Polytechnic Institute, Troy, NY 12180, USA
7. 41% Reduction In Power Stage Area On Silicon-OnInsulator Bipolar-CMOS-DMOS-IGBT Platform With Newly Developed Multiple Deep-Oxide Trench Technology Long , Zhang^{1#}, Jie Ma^{1#}, Yong Gu¹ , Siyang Liu^{1*}, Jiaying Wei¹ , Sheng Li¹ , Weifeng Sun^{1*} and Sen Zhang² ¹ National ASIC System Engineering Research Center, Southeast University, Nanjing, China. *Email: swffrog@seu.edu.cn; liusy2017@seu.edu. ²CSMC Technologies Corporation, Wuxi, China. #These authors contributed equally.
8. GaN Field Emitter Arrays with JA of 10 A/cm² at VGE = 50 V for Power Applications,
P.-C. Shih¹ , T. Zheng² , M. J. Arellano-Jimenez³ , B. Gnade² , A. I. Akinwande¹ , and T. Palacios¹ ¹Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139, USA ²Electrical and Computer Engineering, Southern Methodist University, Dallas, TX, USA ³Department of Materials Science and Engineering, University of Texas at Dallas, Richardson, TX, USA
9. FerroHEMTs: High-Current and High-Speed All-Epitaxial AlScN/GaN Ferroelectric Transistors J. Casamento^{1†} , K. Nomoto^{2†} , T. S. Nguyen¹ , H. Lee² , C. Savant¹ , L. Li² , A. Hickman² , T. Maeda³ , J. Encomendero² , V. Gund² , A. Lal² , J. C. M. Hwang^{1,2} , H. G. Xing^{1,2,3} , and D. Jena^{1,2,3} ¹Department of Materials Science and Engineering, Cornell University, Ithaca, NY 14853, USA, ²School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853, USA ³Kavli Institute at Cornell for Nanoscale Science, Cornell University, Ithaca, NY 14853, USA †Equal Contribution. Email: jac694@cornell.edu, kn383@cornell.edu

10. Record 94 GHz performance from N-polar GaN-on Sapphire MIS-HEMTs: 5.8 W/mm and 38.5% PAE W, Li, B. Romanczyk, E. Akso, M. Guidry, N. Hatui, C. Wurm, W. Liu, P. Shrestha, H. Collins, C. Clymore, S. Keller, and U. K. Mishra University of California Santa Barbara, Santa Barbara, CA, USA, email: weiyili@ucsb.edu
11. First Demonstration of State-of-the-art GaN HEMTs for Power and RF Applications on A Unified Platform with Free-standing GaN Substrate and Fe/C Co-doped Buffer , Mei Wu1,#, Meng Zhang1,#, Ling Yang1,* , Bin Hou1,* , Qian Yu1 , Shiming Li1 , Chunzhou Shi1 , Wei Zhao1 , Hao Lu1 , Weiwei Chen2 , Qing Zhu1 , Xiaohua Ma1,* , and Yue Hao1 1State Key Discipline Lab of Wide Band Gap Semiconductor Technology, Xidian University, Xi'an 710071, China 2China Academy of Space Technology (Xi'an), Xi'an 710100, China *Corresponding authors: yangling@xidian.edu.cn; bhoul@xidian.edu.cn; xhma@xidian.edu.cn. # Authors contributed equally to this work.
12. Terahertz In0.8Ga0.2As quantum-well HEMTs toward 6G applications, Wan-Soo Park1 , Hyeon-Bhin Jo1 , Hyo-Jin Kim1 , Su-Min Choi1 , Ji-Hoon Yoo1 , Ji-Hun Kim1 , Hyeon-Seok Jeong1 , Sethu George1 , Ji-Min Beak1 , In-Geun Lee1 , Tae-Woo Kim2 , Sang-Kuk Kim3 , Jacob Yun3 , Ted Kim3 , Takuya Tsutsumi4 , Hiroki Sugiyama4 , Hideaki Matsuzaki4 , Jae-Hak Lee1 and *Dae-Hyun Kim1 1School of Electronic and Electrical Engineering, Kyungpook National University (KNU), Daegu, South Korea. 2School of Electrical Engineering, University of Ulsan (UoU), Ulsan, South Korea, and 3QSI, Cheon-An, South Korea. 4NTT Device Technology Laboratories, NTT Corporation, Kanagawa, Japan. *E-mail: dae-hyun.kim@ee.knu.ac.kr (Both Park and Jo contributed equally to this work)
13. III-V/III-N technologies for next generation highcapacity wireless communication, N. Collaert, A. Alian, A. Banerjee1 , G. Boccardi, P. Cardinael2 , V. Chauhan1 , C. Desset, R. ElKashlan3 , A. Khaled, M. Ingels, B. Kunert, Y. Mols, B. O'Sullivan, U. Peralagu, N. Pinho, R. Rodriguez, A. Sibaja-Hernandez, S. Sinha, X. Sun, A. Vais, B. Vermeersch, S. Yadav, D. Yan3 , H. Yu, Y. Zhang, M. Zhao, J. Van Driessche, G. Gramegna, P. Wambacq3 , B. Parvais3 and M. Peeters4 Imec, Leuven, Belgium, email: collaert@imec.be 1 Imec, Florida, USA, 2 also UCL, Louvain-la-Neuve, 3 also VUB, Brussels, 4 also University of Antwerp
14. Quantitative study of EOT lowering in negative capacitance HfO2-ZrO2 superlattice gate stacks, M. Hoffmann1* , S. S. Cheema2* , N. Shanker1* , W. Li1 , and S. Salahuddin1 1Electrical Engineering and Computer Sciences, 2Material Sciences and Engineering, University of California, Berkeley, CA, USA email: sayeef@berkeley.edu, *These authors contributed equally to this work.
15. Potential of diamond solid-state quantum sensors M. Hatano1 1 Tokyo Institute of Technology, Meguro, Tokyo, Japan, email: hatano.m.ab@m.titech.ac.jp
16. Thermal Modelling of GaN & InP RF Devices with Intrinsic Account for Nanoscale Transport Effects , B. Vermeersch, R. Rodriguez, A. Sibaja-Hernandez, A. Vais, S. Yadav, B. Parvais1 , and N. Collaert imec, Leuven, Belgium. 1Also at Vrije Universiteit Brussel, Brussels, Belgium. Email: bjorn.vermeersch@imec.be
17. Steep-Slope Negative Quantum Capacitance FieldEffect Transistor , Yafen Yang1 , Kai Zhang1 , Yi Gu1 , Parameswari Raju2,3 , Qiliang Li2,3,* , Li Ji1 , Lin Chen1 , Dimitris E. Ioannou3 , Qingqing Sun1 , David Wei Zhang1 , and Hao Zhu1,* 1School of Microelectronics, Fudan University, Shanghai, China, email: hao_zhu@fudan.edu.cn 2Engineering Physics Division, National Institute of Standards and Technology, Gaithersburg, MD, USA, email: qiliang.li@nist.gov 3Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA, USA
18. Enabling Next Generation 3D Heterogeneous Integration Architectures on Intel Process , A. Elsherbini(1), K. Jun(1), S. Liff(3), T. Talukdar(1), J. Bielefeld(1), W. Li(1), R. Vreeland(1), H. Niazi(2), B. Rawlings(1), T. Ajayi(2), N. Tsunoda(2), T. Hoff(1), C. Woods(2), G. Pasdast(5), S. Tiagaraj(5), E. Kabir(4), Y. Shi(2), W. Brezinski(1), R. Jordan(1), J. Ng(3), X. Brun(2), B. Krisnatreya(6), P. Liu(4), B. Zhang(2), Z. Qian(2), M. Goel(7), J. Swan(1), G. Yin(3), C. Pelto(3), J. Torres(1), P. Fischer(1) (1)Components Research, (2)Assembly and Test Technology Development, (3)Logic

Technology Development, (4)Corporate Quality Network, (5)Design Engineering Group, (6)Global Sourcing for Equipment and Materials, (7)Design Enabling Group, Intel Corporation, USA. Email: adel.a.elsherbini@intel.com

19. Back Barrier Trapping Induced Resistance Dispersion in GaN HEMT: Mechanism, Modeling, and Solutions , Hao Yu1,* , B. Parvais1,2 , U. Peralagu1 , R. Y. ElKashlan1,2 , R. Rodriguez1 , A. Khaled1 , S. Yadav1 , A. Alian1 , M. Zhao1 , N. de Almeida Braga3 , J. Cobb3 , J. Fang3 , P. Cardinael1,4 , A. Sibaja-Hernandez1 , and N. Collaert1 1 imec, Leuven, Belgium 2 also with Vrije Universiteit Brussel, Brussels, Belgium 3Synopsys, California, US 4 also with Université catholique de Louvain, Louvain-la-Neuve, Belgium *Tel: +32(16)1811, Email: hao.yu@imec.be

20. Novel all-around diamond integration with GaN HEMTs demonstrating highly efficient device cooling , R. Soman1 , M. Malakoutian1 , B. Shankar1 , D. Field2 , E. Akso 3 , N.Hatui3 , N. J. Hines4 , S. Graham5 , U. K. Mishra3 , M. Kuball 2 , and S. Chowdhury1

21. Comprehensive Investigations of HBM ESD Robustness for GaN-on-Si RF HEMTs, S. Abhinay1,2*, W.-M. Wu1,2,3*, C.-A. Shih1,3, S.-H. Chen1 , A. Sibaja-Hernandez1 , B. Parvais1,4, U. Peralagu1 , A. Alian1 , T.-L. Wu3 , M.-D. Ker3 , G. Groeseneken1,2, N. Collaert1 1 imec, Kapeldreef 75, 3001 Leuven, Belgium, email: sandup54@imec.be, 2Electrical Engineering (ESAT), KU Leuven, Belgium, 3National Yang Ming Chiao Tung University, Taiwan, 4VUB, Brussels, Belgium, * equal contribution

22. Analog Computing in Memory (CIM) Technique for General Matrix Multiplication (GEMM) to Support Deep Neural Network (DNN) and Cosine Similarity Search Computing using 3D AND-type NOR Flash Devices

Ming-Liang Wei1,2, Hang-Ting Lue1 , Shu-Yin Ho1 , Yen-Po Lin1,2, Tzu-Hsuan Hsu1 , Chih-Chang Hsieh1 , Yung-Chun Li1 , Teng-Hao Yeh1 , Shih-Hung Chen1 , Yi-Hao Jhu1 , Hsiang-Pang Li1 , Han-Wen Hu1 , Chun-Hsiung Hung1 , Keh-Chung Wang1 , and Chih-Yuan Lu1 1. Macronix International Co., Ltd 16 Li-Hsin Road, Hsinchu Science Park, Hsinchu, Taiwan. 2. Graduate Institute of Electronic

23. An Analog In-Memory-Search Solution based on 3D-NAND Flash Memory for Brain-Inspired Computing , Po-Hao Tseng* , Yu-Hsuan Lin, Tian-Cih Bo, Feng-Ming Lee, Yu-Yu Lin, Ming-Hsiu Lee, Kuang-Yeu Hsieh, Keh-Chung Wang, and Chih-Yuan Lu Macronix International Co., Ltd., 16 Li-Hsin Rd. Hsinchu Science Park, Hsinchu, Taiwan, ROC TEL: +886-3-5786688 ext. 78024, Email: pohaotseng@mxic.com.tw

24. CMOS Demonstration of Negative Capacitance HfO₂- ZrO₂ Superlattice Gate Stack in a Self-Aligned, Replacement Gate Process , N. Shanker1* , M. Cook2* , S.S. Cheema1* , W. Li1* , , R. Rastogi2 , D. Pipitone2 , C. Chen2 , M. Smith2 , S. Meninger2 , F. Bauer2 , G. Pinelli2 , J. Hunt2 S. Salahuddin1 , M. Mohamed2 1 Department of Electrical Engineering and Computer Sciences, University of California, Berkeley 2 Lincoln Laboratory, Massachusetts Institute of Technology * These authors contributed equally; email: Mohamed.mohamed@ll.mit.edu

25. Scaled Submicron Field-Plated Enhancement Mode High-K Gallium Nitride Transistors on 300mm Si(111) Wafer with Power FoM (RONxQGG) of 3.1 mohm-nC at 40V and fT/fMAX of 130/680GHz , HanWuiThen, M. Radosavljevic, P. Koirala, M. Beumer, S. Bader, A. Zubair, T. Hoff, R. Jordan, T. Michaelos, J. Peck, I. Ban, N. Nair, H. Vora, K. Joshi, I. Meric, A. Oni, N. Desai, H. Krishnamurthy, K. Ravichandran, J. Yu, S. Beach, D. Frolov, A. Hubert, A. Latorrey, S. Rami, J. Rangaswamy, Q. Yu, P. Fischer Components Research, Intel Corporation, Hillsboro, OR 97124, USA. Email: han.wui.then@intel.com

26. 1200V GaN Switches on Sapphire: A low-cost, highperformance platform for EV and industrial applications , G. Gupta1 , M. Kanamura2 , B. Swenson1 , C. Neufeld1 , T. Hosoda2 , P. Parikh1 , R. Lal1 , U. Mishra1 1Transphorm, Inc., Goleta-CA, USA, email: ggupta@transphormusa.com 2Transphorm Japan, Shin-Yokohama, Japan

27. Highly-Scaled Self-Aligned GaN Complementary Technology on a GaN-on-Si Platform , Qingyun Xie1*† , Mengyang Yuan1† , John Niroula1 , James A. Greer1 , Nitul S. Rajput2 , Nadim Chowdhury3,1* , and Tomás Palacios1* 1Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139,

U.S.A. 2Advanced Materials Research Center, Technology Innovation Institute, Abu Dhabi P.O. Box 9639, United Arab Emirates 3Dept. of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka-1205, Bangladesh * e-mail: qyxie@mit.edu, nadim@eee.buet.ac.bd, tpalacios@mit.edu (+ equal contribution)

28. Hybrid Gate p-GaN Power HEMTs Technology for Enhanced Vth Stability , Chi Zhang¹ , Sheng Li¹ , Siyang Liu^{1*}, Weihao Lu¹ , Yanfeng Ma¹ , Jiaying Wei¹ , Long Zhang¹ , Weifeng Sun^{1*}, Denggui Wang² , Jianjun Zhou² and Song Bai² ¹National ASIC System Engineering Research Center, Southeast University, Nanjing, Jiangsu, China, ²Nanjing Electronic Devices Institute, Nanjing, Jiangsu, China, *Email: liusy2017@seu.edu.cn; swffrog@seu.edu.cn

29. Superior Breakdown, Retention, and TDDDB Lifetime for Ferroelectric Engineered Charge Trap Gate E-mode GaN MIS-HEMT , J.-S. Wu, P.-H. Liao, S.-J. Chang, T.-Y. Yang, C.-Y. Teng, Y.-K. Liang, D. Panda, Q. H. Luc, and E. Y. Chang National Yang Ming Chiao Tung University, Hsinchu, Taiwan. E-mail: edc@nycu.edu.tw

30. First Demonstration of Vertical Superjunction Diode in GaN , Ming Xiao^{1ξ} * , Yunwei Ma^{1ξ*}, Zhonghao Du² , Yuan Qin¹ , Kai Liu³ , Kai Cheng³ , Florin Udrea⁴ , Andy Xie⁵ , Edward Beam⁵ , Boyan Wang¹ , Joseph Spencer^{1,6}, Marko Tadjer⁶ , Travis Anderson⁶ , Han Wang^{2*}, Yuhao Zhang^{1*} ¹ Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, Blacksburg, VA USA ² Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, CA USA ³ Enkris Semiconductor, Inc., Suzhou, Jiangsu China ⁴ Department of Engineering, University of Cambridge, Cambridge UK ⁵ Qorvo, Inc., Richardson, TX USA ⁶ U.S. Naval Research Laboratory, Washington, DC USA ^ξ The two authors contributed equally to this work. *Email: {mxiao, yunwei, yhzhang}@vt.edu, han.wang.4@usc.edu

31. Current Status and Future Prospects of GaN-on-GaN Vertical Power Devices J. Suda^{1,2} ¹ Department of Electronics, Nagoya University, Nagoya, Japan, email: suda@nuee.nagoya-u.ac.jp ² Institute of Materials and Systems for Sustainability, Nagoya University, Nagoya, Japan