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A Fully-Blind Fractionally-Oversampled Frequency Domain Adaptive Equalizer

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Abstract: A frequency domain adaptive equalizer, operating with fewer than 2 Sa/Symbol is investigated. Steady state performance and dynamic operation are demonstrated without equalizer training. We find that the equalizer exhibits no penalty as low as 1.1 Sa/Symbol.

OCIS codes: (060.4510) Optical communications, (060.1660) Coherent communication.

1. Introduction

Digital coherent systems are now standardized for high-capacity optical networks. Coherent receivers together with analog-to-digital converters (ADC) are able to translate the entire optical field into the digital domain and allow the use of effective digital signal processing (DSP) to mitigate optical impairments and reduce optical complexity. To accommodate the increasing bandwidth demands, line rates beyond 400 Gbit/s are now being investigated. However, these systems require high-power and high-bandwidth ADCs that can support multi-level modulation formats. To tackle these problems algorithms that can operate at lower than 2 Sa/Symbol have been investigated recently [1–5]. By utilizing ADCs at lower sample rate power consumption can be reduced for those components and they can be used to detect higher symbol rates, limited by the electrical bandwidth and Nyquist’s sampling criterion. Additionally, as part of the digital processing can be performed at a lower sample rate, fewer samples are processed which minimizes the computational complexity and further lowers power consumption.

Previous work has mostly focused on either interpolating the lower sampled signal prior to equalization [1, 2] or as part of a time domain equalizer (TDE) utilizing filter banks [5], which do not decrease the complexity significantly. More recently a frequency domain equalization (FDE) where re-sampling is performed as part of the equalization has been demonstrated [4]. However, adaptation in [4] requires a periodic training sequence, thus lowering throughput and channel tracking capability.

In this work we analyze and compare the complexity of a blind fractionally spaced FDE scheme with existing interpolation scheme with TDE, demonstrating significant reduction. Furthermore, we investigate the both steady state performance and polarization rotation tolerance of the scheme at different sample rates and compare it to existing techniques, with no performance degradation observed.

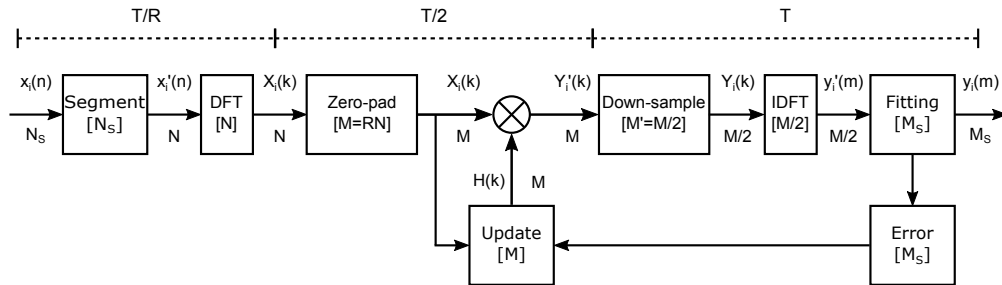


Fig. 1: The structure of fractionally spaced frequency domain equalizer, $R = (Sa/Symbol)/2$.

2. Proposed Equalizer Structure

The structure of the proposed equalizer is illustrated in figure 1, where a conventional FDE utilizing an overlap-save is interleaved with a frequency domain interpolation. At the input of the equalizer, the signal is segmented into blocks, with a 50% overlap. Each block then undergoes an N -point ($N = 2N_s$) Discrete Fourier Transform (DFT), before processing in the frequency domain. A 2×2 butterfly structure is used in the frequency domain to perform polarization demultiplexing and equalization. Although the length of block is M , due to zero-padding only N of the multiplication

are non-zero, and the remainder do not have to be computed. The signal is then down-sampled by a factor 2, resulting in symbol rate sampling, before transforming it to the time domain using an inverse DFT and discarding the 50% overlap, M_S , *Fitting*. The equalizer errors are calculated on the output symbols and transformed to the frequency domain where they are up-sampled to 2 Sa/Symbol and constraint [6]. In this work M is set to be a power of two allowing for a Fast Fourier Transforms (FFT) to be used for the error vector transforms and to transform the equalized signal to the time domain. By choosing the length M , the input length of N was fixed such that $N = M/R$.

In the proposed configuration the CD compensation would be performed separately prior to equalization using conventional design methods at lower sample rate as previously demonstrated [1]. This allows the equalizer to utilize shorter filter lengths which can more easily converge and eliminate the need for training sequences.

The computational complexity for a CD compensation and conventional equalization schemes per output symbol is summarized in figure 2(a). The following configuration are considered in figure 2(b); conventional DSP with 2 Sa/Symbol CD compensation and TDE or FDE, a CD compensation operating a fewer than 2 Sa/Symbol followed by conventional equalizer and finally the proposed scheme with where both the CD compensation the equalization are performed with less than 2 Sa/Symbol. The interpolation before the equalizer can be performed using a Farrow filter [7], which will be present in all the DSP configurations for clock recovery through a feedback loop from the equalizer. The complexity of the Farrow filter is low and largely independent of sampling rate and is therefore omitted in the complexity calculations. Only the filtering complexity of the equalizer is considered as the complexity of the equalizer update will depend on the update rate. From figure 2(b) it is observed that the largest complexity reduction comes from utilizing a FDE over TDE especially for longer equalizer filters. Additionally a large complexity reduction is achieved from applying a CD compensation at lower than 2 Sa/Symbols and further reduction is realized when the equalizer is also operates at a lower sample rate. The complexity is dependent on the sampling rate and converges to the expected value as the sampling rate increased to 2 Sa/Symbol. In figure 2(b) the complexity is plotted for sample rate of 1.1 Sa/Symbol and with accumulated CD of 17000 ps/nm at 28 GBd.

	Complex Multiplications
CD(2 Sa)	$4N_{CD} + 8N_{CD} \log_2(2N_{CD})$
CD(2R Sa)	$4N_{CD}R^2 + 8N_{CD}R^2 \log_2(2N_{CD}R^2)$
TDE(2 Sa)	$4N$
FDE(2 Sa)	$8N + 4N \log_2(2N) + 2N \log_2(N)$
FDE(2R Sa)	$8NR + 4NR \log_2(2NR) + 2N \log_2(N)$

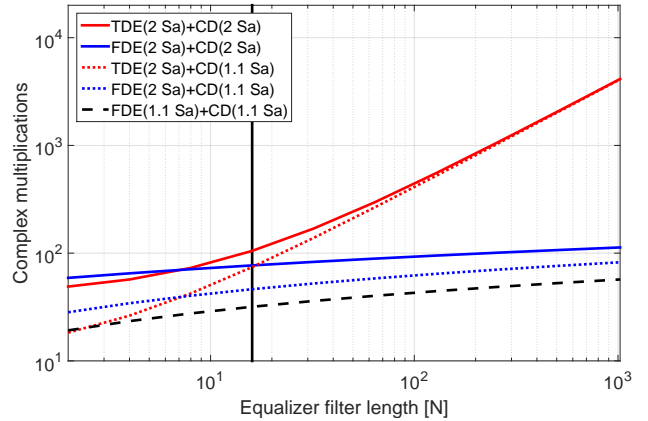


Fig. 2: Computational complexity of equalizer filter per output symbol with different implementations, N -equalizer taps, $R = (Sa/Symbol)/2$. **a)** Analytical complexity. **b)** Complexity for 1.1 Sa/Symbol and 17000 ps/nm of CD at 28 GBd, $N_{CD} = 854$. The vertical line indicates 16 tap equalizer.

3. Simulation Setup

To verify the performance of the equalizer, 28 GBd Polarization Division Multiplexed Quadrature Phase Shift Keying (PDM-QPSK) was simulated. The signal was generated at 2 Sa/Symbol and filtered with a Root Raised Cosine (RRC) filter with a roll-off of 10% implemented with 32 taps. Additionally two 5th order Bessel filters with a bandwidth of 19.6 GHz were used to emulate the electronic bandwidth of the transmitter and receiver. Although CD compensation was not considered in this work, 510 ps/nm ($N_{CD} = 13$), was introduced to verify that the equalizer can tolerate residual dispersion. The signal was then noise loaded or polarization rotations with a constant speed were added before being detected and down-sampled to different sampling rates. At the receiver no RRC filter was applied, instead the equalizer was allowed to converge to correct impulse response. After equalization symbol detection and error counting was performed.

4. Results

First the steady state performance of the equalizer was investigated, illustrated in figure 3(a). It is clear that the equalizer performance is independent of the sampling rate and is equivalent to the conventional 2 Sa/Symbol FDE. Afterwards, polarization rotation tolerance was explored for fixed OSNR of 13 dB and fixed filter length of 16 taps (the complexity of which is marked with a the vertical line in figure 2(b)). The convergence parameter was fixed at $\mu = 2 \cdot 10^{-2}$, and the equalizer taps were updated every block. The results are presented in figure 3(b) where the performance is measured in Q-factor penalty compared to the steady state. A small variation is observed between the different sampling rate which is attributed to the fact that higher sampling rates have less zero-padding and more active taps. This ultimately results in a slightly larger effective convergence parameter across the processed block and higher tolerance to polarization rotations. Additionally, the tolerance for larger filter length, 128 taps, is also shown to illustrate a potential challenge when CD and equalization is merged into a single stage with a large filter length as previous proposed [4]. The tolerance to polarization rotations is decreased by almost an order of magnitude.

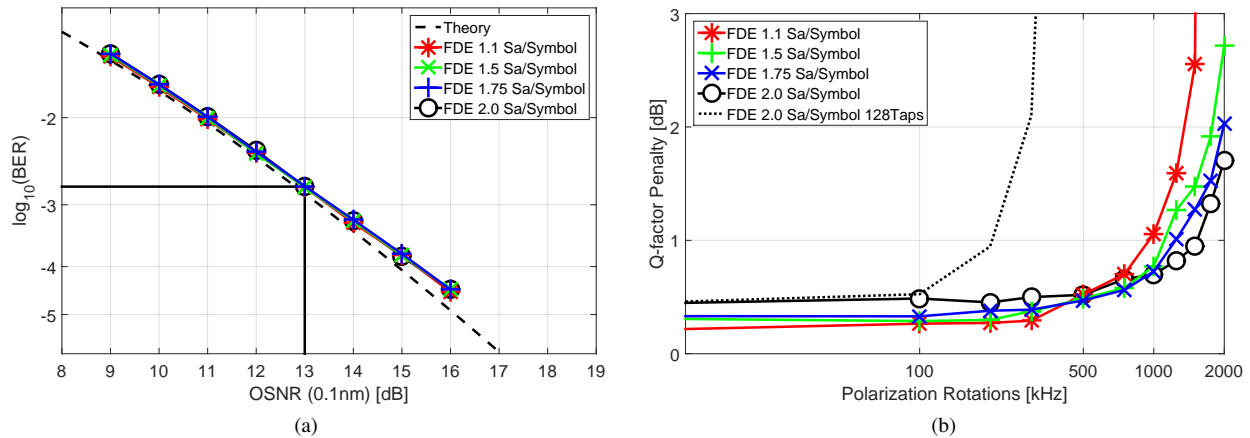


Fig. 3: PDM-QPSK 28 GBd equalized with 16 taps: **a)** BER vs OSNR with different sampling rates. **b)** Penalty vs polarization rotations at an OSNR of 13 dB with a fixed convergence parameter $\mu = 2 \cdot 10^{-2}$

5. Conclusions

We have proposed a fully blind FDE structure operating at a sample rates less than 2 Sa/Symbol. Steady state and dynamic performance were analyzed, with no performance penalty observed at 1.1 Sa/Symbol. By allowing the signal to be processed at a lower rate reduced computational complexity can be achieved leading to power saving and the ability to detect signals with higher symbol rates.

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